Using 28F128J3D Flash on the phyCORE-PXA255 / phyCORE-PXA270

Application Note

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Preface

This Application Note describes how to use Intel® 28F128J3D Embedded Flash memory populating the phyCORE-PXA255 or the phyCORE-PXA270.

Initial phyCORE-PXA modules were populated with 28F128K3 Intel Strata Flash devices. Due to changes with the Intel Flash µBGA packaging PHYTEC switched to the 28F128J3D Embedded Flash memory on new production runs.

For general startup instructions of your phyCORE-PXA255 (PCM-022) / phyCORE-PXA270 (PCM-027) please refer to the phyCORE-PXA255 and phyCORE-PXA270 Hardware Manuals. Precise specifications for Intel's PXA255 and PXA270 controller can be found in the corresponding Data Sheet/User's Manual.

1 PXA270 Register Settings for 28F128J3D Flash

1.1 Core Clock Configuration Register (CCCR)

The PXA270 processor contains a Clock Manager to manage its multiple clock sources. The optimal CLK_MEM frequency for the phyCORE-PXA270 is 104.00 MHz.

Recommended configuration of:

CCCR:L[4:0] = 0b 01000 Multiplier = 8 * 13.000 MHz

1.2 Static Memory Control Register

Chip Select /CS_0 from the PXA270 processor controls the on-board Flash device. The data bus width is 32-bits. The asynchronous 28F128J3D Flash only support 4-word page-mode reads.

Recommended configuration of:

MSC0[15..0] = 0001 0010 1010 0010

Name	Bit(s)	Value (b)	Description
RBUFF0	[15]	0	Slower devices
RRR0	[14:12]	001	2 CLK_MEM cycles read recovery
RDN0	[11:8]	0010	3 CLK_MEM next access delay
RDF0	[7:4]	1010	12 CLK_MEM first access delay, 11 CLK_MEM for subsequent access
RBW0	[3]	0	32 data bits
RT0	[2:0]	010	Burst-of-four Flash

Table 1: MSC0 Bit Definitions and Settings for PXA270

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2 PXA255 Register Settings for 28F128J3D Flash

2.1 Core Clock Configuration Register (CCLKCFG)

The PXA255 processor contains a Clock Manager to manage its multiple clock sources. The optimal CLK_MEM frequency for the phyCORE-PXA270 is 99.53 MHz.

Recommended configuration of:

CCLKCFG:L[3:0] = 0b 0001;
Multiplier = 27 (Turbo Mode) * 3.686 MHz (on-board quartz frequency)

2.2 Static Memory Control Register

Chip Select /CS_0 from the PXA255 processor controls the on-board Flash device. The data bus width is 32-bits. The asynchronous 28F128J3D Flash only support 4-word page-mode reads.

Recommended configuration of:

MSC0[15..0] = 0b 0001 0010 1010 0010

Name	Bit(s)	Value (b)	Description
RBUFF0	[15]	0	Slower devices
RRR0	[14:12]	001	2 CLK_MEM cycles read recovery
RDN0	[11:8]	0010	3 CLK_MEM next access delay
RDF0	[7:4]	1010	12 CLK_MEM first access delay, 11 CLK_MEM for subsequent access
RBW0	[3]	0	32 data bits
RT0	[2:0]	010	Burst-of-four Flash

Table 2: MSC0 Bit Definitions and Settings for PXA255

3 Configuration of U-boot Loader

3.1 U-boot Modification for phyCORE-PXA270

Follow the steps below to create a new U-boot image supporting the new Intel Flash devices populating the phyCORE-PXA270:

- Open the file ……..\u-boot-1.1.3\include\configs**PCM027.h**
- Use the following setting for typical 28F128J3D Flash timing:
  #define CFG_MSC0_VAL 0x128C12A2
- Change the Flash UNLOCK setting:
  #undef CFG_FLASH_UNLOCK
- Create a new u-boot image

3.2 U-boot Modification for phyCORE-PXA255

Follow the steps below to create a new U-boot image supporting the new Intel Flash devices populating the phyCORE-PXA255:

- Open the file ……..\u-boot-1.1.3\include\configs**PCM022.h**
- Setting for 28F128J3D typical Flash timing
  #define CFG_MSC0_VAL 0x12AA12A2
- Change the Flash UNLOCK setting
  #undef CFG_FLASH_UNLOCK
- Create a new u-boot image.

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