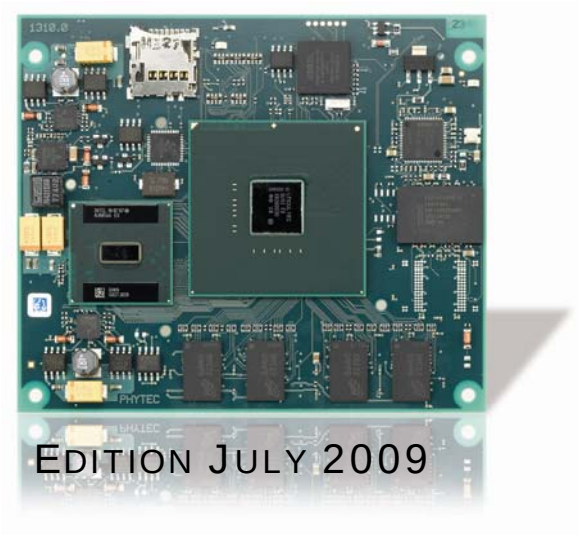
PHYTEC

phyCORE-Z500P(T)

ATOM®

Preliminary

HARDWARE MANUAL



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1 Preface

This phyCORE-Z500PT Hardware Manual describes the single board computer's design and functions. Precise specifications for the Intel® Z500PT CPU/Chipset can be found in the enclosed microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" or "#" preceding the signal name (i.e.: /RD or #RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformity of the PHYTEC phyCORE-Z500PT

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-Z500PT is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market. For more information go to:

http://www.phytec.com/services/phytec-advantage.html

1.1 Introduction

The phyCORE-Z500PT belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled Microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-Z500PT is a subminiature (85 x 100 mm) insert-ready Single Board Computer populated with the Intel® Atom Z510P/PT, Z520PT or Z530P CPU. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to a high-density pitch (0.5 mm) connector aligning on one side of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or datasheet. The descriptions in this manual are based on the Intel® Z500PT. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-Z500PT.

The phyCORE-Z500PT offers the following features:

- Subminiature Single Board Computer (85 x 100 mm) achieved through modern SMD technology
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- Controller signals and ports extend to one 2 x 120-pin high-density (0.5 mm) Samtec connector aligned one side of the board, enabling it to be plugged like a "big chip" into target application
- Populated with the Intel® Atom Z510P/PT, Z520PT or Z530P microprocessor (packaging 437-ball, µFCBGA8 22 x 22 mm)
- System Controller Hub, US15WP/WPT
- DDR2 RAM up to 2GB (Kitversion with 512 MB)
- Solide State Disc (SSD) up to 16GB (Kitversion with 2 GB)
- Intel® 82574 Ethernet controller with 10/100/1000 Mbit/s
- 8 x USB2.0 (6 x Low-/Full-/High-Speed, 2 x HighSpeed only)
- microSD slot on board
- SATA interface (Master / Slave)
- 2 x PCIexpress lanes (On the baseboard an additional PCIexpress switch is populated offering access to two PCIe x 1, 1 miniPCIe and an Altera Aria-GX FPGA)
- 3 x SDIO port
- LVDS Display interface (18-/ 24-bit)
- SDVO Display interface
- System Management Bus (SMB)
- Low Pin Count Bus (LPC Bus)
- 5 Volt Single Supply
- Physical dimensions: 85 x 100 mm
- Temperature Range:
  - o standard: 0...+70°C
  - o extended: -40...+85°C

1.2 Block Diagram

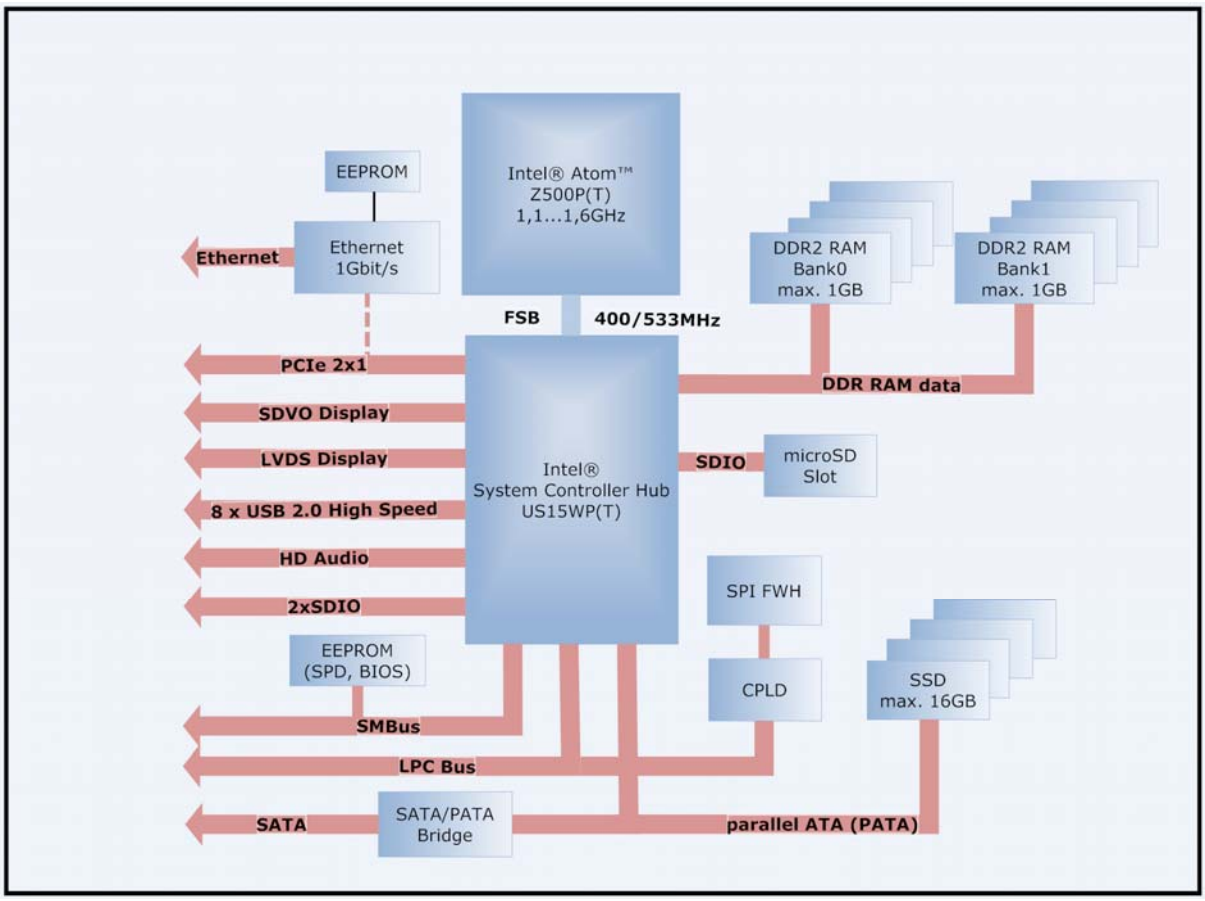


Figure 1: Block Diagram phyCORE-Z500PT

1.3 View of the phyCORE-Z500PT

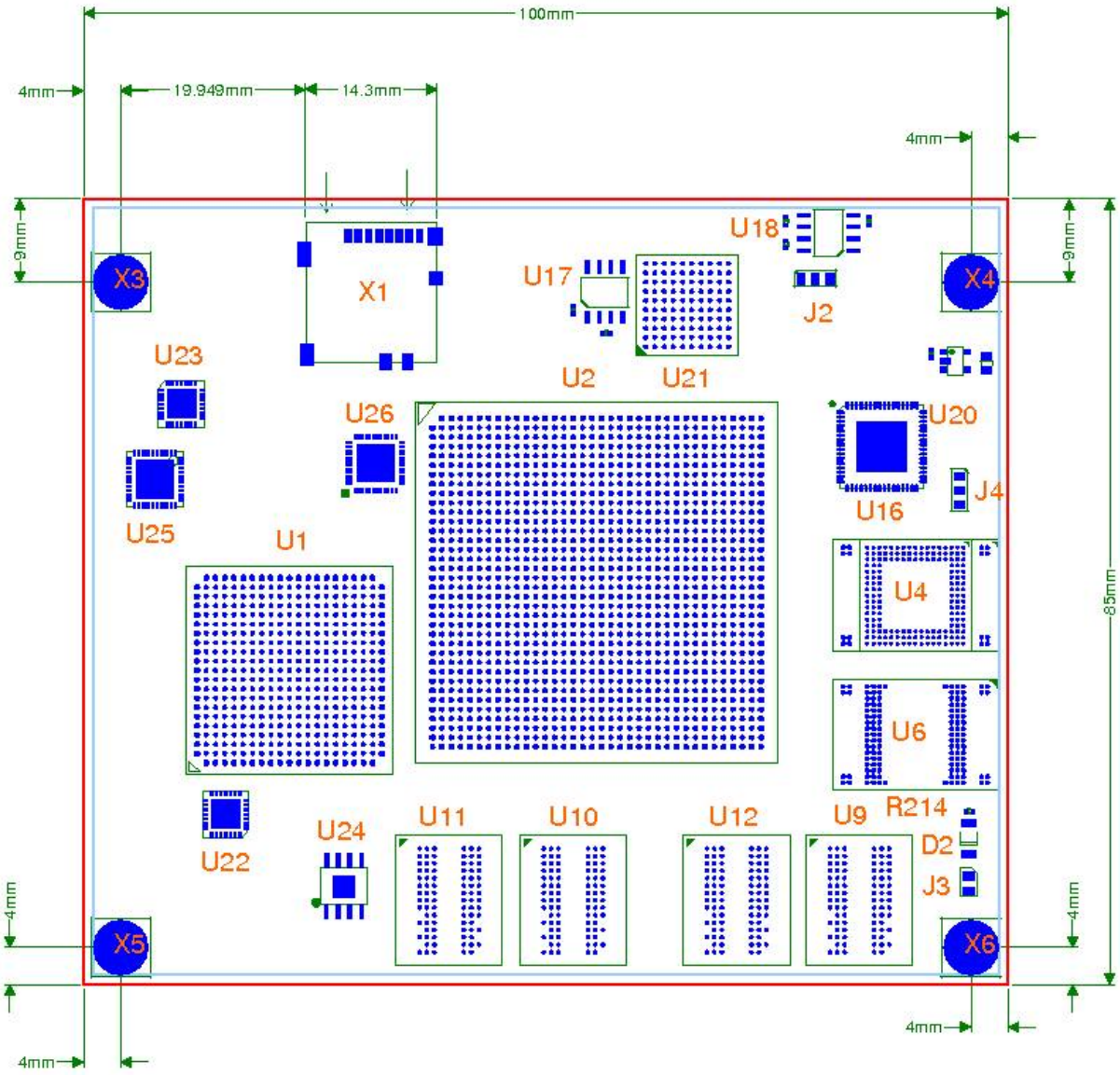


Figure 2: Top View of the phyCORE-Z500PT (controller side)

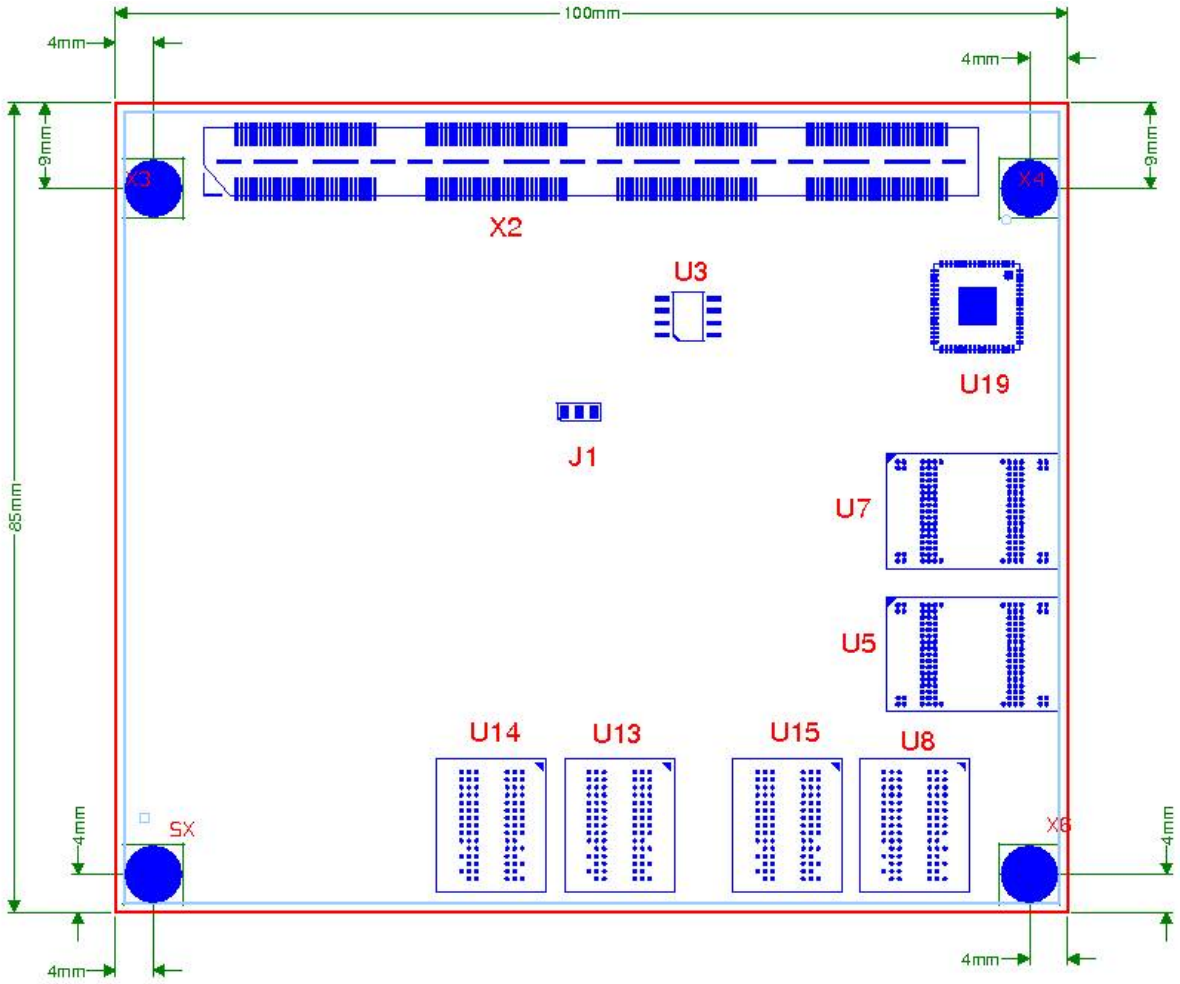


Figure 3: Bottom View of the phyCORE-Z500PT (connector side)

2 Pin Description (X2)

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Table 1* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.5 mm) on one side of the module (referred to as phyCORE-connector). This allows the phyCORE-Z500P(T) to be plugged into any target application like a "big chip".

The connector used on the phyCORE-Z500P(T) is a QSH-120-01-L-D-A from Samtec.

QSH-120-01-L-D-A

The mating connector, for the baseboard, is

QTH-120-01-L-D-A

Table 1 provides an overview of the pinout of the phyCORE-connector, as well as descriptions of possible alternative functions. *Table 1* also provides the appropriate signal level interface voltages listed in the SL (**S**ignal **L**evel) column. The Intel® Z500PT is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. *Please refer to the Intel® Z500PT User's Manual/Data Sheet for details on the functions and features of controller signals and port pins*.

NOTE:
SL is short for Signal Level (V) and is the applicable logic level to interface a given pin. Those pins marked as “N/A” have a range of applicable values that constitute proper operation.

Table 1: Pinout of the phyCORE-Connector X2

Pin	Name	Description	Type
1,3,5,7,9	VCC5VA	Main Power Supply	Power
11	GND	Ground	Power
13	HDA_SDI_0		
15	HDA_SDI_1		
17	#HDA_DOCKEN		
19	HDA_DOCKRST		
21	HDA_RST		
23	FWH_BSEL		Bankselect input for BIOS backup
25	FWH_EN	Disable on board FWH	Input (PU)
27	#SMI	System Managment Interrupt	
29	#PM_SLP_S3	S3 control-signal	output
31	#PM_SLP_S4	S4 control-signal	output
33	#H_INIT		
35	SMB_CLK	System-Managment-Bus Clock	
37	SMB_DATA	System-Managment-Bus Data	Bidir (PU)
39	CLK_LPC_PORT80	LPC Clock used for Port 80	output
41	GND	Ground	Power
43	CLK_LPC_FWH	LPC Clock for FWH	output
45	LPC_FRAME	LPC Frame Signal	
47	#LPC_CLKRUN	LPC....	
49	LPC_SERIRQ	LPC interrupt line	
51	GND	Ground	Power
53	GPIO_SUS0		
55	#PM_PWRBTTN	Debounced copy of #SMC_ONOFF	output
57	GPIO_0		IO
59	GPIO_2		IO
61	GND	Ground	Power
63	GPIO_4		IO
65	GPIO_6		IO
67	GPIO_8		IO
69	#H_IERR		
71	GND	Ground	Power
73	MMC_0_LED	Activity output MMC0	output
75	#MMC0_CD	Card detect MMC0	Input (PU)

77	MMC0_WP	Write protect MMC0	input
79	#MMC0_PWR	Power enable output MMC0	output
81	GND	Ground	Power
83	MMC0_CLK	Clock MMC0	output
85	MMC0_CMD	Command MMC0	bidir
87	MMC0_DATA0	MMC0 dataline 0	bidir
89	MMC0_DATA1	MMC0 dataline 1	bidir
91	GND	Ground	Power
93	MMC0_DATA2	MMC0 dataline 2	bidir
95	MMC0_DATA3	MMC0 dataline 3	bidir
97	MMC1_LED	Activity output MMC1	output
99	#MMC1_CD	Card detect MMC1	input
101	GND	Ground	Power
103	MMC1_WP	Write protect MMC1	Input
105	#MMC1_PWR	Power enable output MMC1	Output
107	MMC1_CMD	Command MMC1	Bidir
109	MMC1_CLK	Clock MMC1	Output
111	GND	Ground	Power
113	MMC1_DATA2	MMC1 dataline 2	Bidir
115	PLD_TDO	TDO from PLD	Output (PU/3V3)
117	PLD_TDI	TDI from PLD	Output (PU/3V3)
119	PLD_TCK	TCK from PLD	Input
121	GND	Ground	Power
123	PLD_TMS	TMS from PLD	Input
125	XDP_TRST	TRST from CPU	Input
127	XDP_TCK_0	TCK from CPU	Input
129	#USB_OC_7	Over current USB port 7	Input
131	USB_DP_7	USB Port 7 pos. Dataline	Diff. Bidir
133	USB_DN_7	USB Port 7 neg. Dataline	Diff bidir
135	#USB_OC_6	Over current USB port 6	Input
137	GND	Ground	Power
139	USB_DP_6	USB Port 6 pos. Dataline	Diff bidir
141	USB_DN_6	USB Port 6 neg. Dataline	Diff bidir
143	#USB_OC_3	Over current USB port 3	Input
145	USB_DP_3	USB Port 3 pos. Dataline	Diff bidir
147	USB_DN_3	USB Port 3 neg. Dataline	Diff bidir
149	GND	Ground	Power
151	USB_DP_2	USB Port 2 pos. Dataline	Diff bidir
153	USB_DN_2	USB Port 2 neg. Dataline	Diff bidir
155	#USB_OC_2	Over current USB port 2	input

157	USB_DP_0	USB Port 0 pos. Dataline	Diff bidir
159	USB_DN_0	USB Port 0 neg. Dataline	Diff bidir
161	GND	Ground	Power
163	#USB_OC_0	Over current USB port 0	input
165	LA_DATAP_0	LVDS data group 0 pos. signal	Diff output
167	LA_DATAM_0	LVDS data group 0 neg. signal	Diff output
169	L_DDC_CLK	DDC clock	Output (PU)
171	LA_DATAP_1	LVDS data group 1 pos. signal	Diff output
173	LA_DATAM_1	LVDS data group 1 neg. signal	Diff output
175	GND	Ground	Power
177	LA_DATAP_3	LVDS data group 3 pos. signal	Diff output
179	LA_DATAM_3	LVDS data group 3 neg. signal	Diff output
181	SMC_SHUTDOWN	...	output
183	L_BKLTEN	LCD Backlight enable	output
185	SDVO_TVCLKIN	SDVO TVCLKIN pos. signal	
187	#SDVO_TVCLKIN	SDVO TVCLKIN neg. signal	
189	GND	Ground	Power
191	SDVO_CTRLCLK	SDVO management clock	Output (PU)
193	SDVOB_STALL	SDVOB STALL pos. signal	
195	#SDVOB_STALL	SDVOB STALL neg. signal	
197	GND	Ground	Power
199	MDI_PLUS0	Ethernet MDI0 pos. signal	Diff bidir
201	MDI_MINUS0	Ethernet MDI0 neg. signal	Diff bidir
203	LAN_LED0	Ethernet Activity Led	Output (OD)
205	MDI_PLUS1	Ethernet MDI1 pos. signal	Diff bidir
207	MDI_MINUS1	Ethernet MDI1 neg. signal	Diff bidir
209	GND	Ground	Power
211	MDI_PLUS2	Ethernet MDI2 pos. signal	Diff bidir
213	MDI_MINUS2	Ethernet MDI2 neg. signal	Diff bidir
215	LAN_LED1	Ethernet Link Led	Output (OD)
217	MDI_PLUS3	Ethernet MDI3 pos. signal	Diff bidir
219	MDI_MINUS3	Ethernet MDI3 neg. signal	Diff bidir
221	GND	Ground	Power
223	CLK_PCIE_SLOT0_CON	PCIe pos. clock for Slot 0	Diff output
225	#CLK_PCIE_SLOT0_CON	PCIe neg. clock for Slot 0	Diff output
227	#PCIE_WAKE	Wake Signal	input
229	GND	Ground	Power
231	PCIE_TXP_1_CON	First PCIe Transmit pos.	Diff output
233	#PCIE_TXN_1_CON	First PCIe Transmit neg.	Diff output
235	#CLK_SLOT0_OE	Output enable for Slot 0 clock	Input (PU)

237	PCIE_RXP_1_CON	First PCIe receive pos.	Diff input
239	PCIE_RXN_1_CON	First PCIe receive neg.	Diff input
2,4,6,8,10	VCC5VA	Main Power Supply	Power
12	GND	Ground	Power
14	VBAT	3V3 Coin-Cell for CMOS	Power
16	HDA_CLK		
18	HDA_SDO		
20	HDA_SYNC		
22	HDA_SPKR		
24	#SMC_RST	Main-Reset Input	
26	#SMC_ONOFF	Input for Power Button	Input (PU)
28	#SMC_RUNTIME_SCI		
30	#PM_SYSRST		output
32	#PM_THRM		
34	#PM_THERMTRIP		
36	#H_A20M		
38	#SMB_ALERT	System-Managment-Bus Alert	Input (PU)
40	CLK_LPC_TPM	LPC Clock for TPM	output
42	GND	Ground	Power
44	LPC_AD0	LPC Bus Address 0	
46	LPC_AD1	LPC Bus Address 1	
48	LPC_AD2	LPC Bus Address 2	
50	LPC_AD3	LPC Buss Address 3	
52	GND	Ground	Power
54	#L_BKLTSEL_0_GPIO	LVDS Backlight select / GPIO	
56	SCH_GPIOSUS_3		
58	GPIO_1		IO
60	GPIO_3		IO
62	GND	Ground	Power
64	GPIO_5		IO
66	#SLPIOVR		
68	#L_BKLTSEL	LVDS Backlight select	output
70	#H_IGNNE		
72	GND	Ground	Power
74	MMC_2_LED	Activity output MMC2	output
76	#MMC2_CD	Card detect MCM2	Input (PU)
78	MMC2_WP	Write protect MMC2	input

80	#MMC2_PWR	Power enable output MMC2	output
82	GND	Ground	Power
84	MMC2_CLK	Clock MMC2	output
86	MMC2_CMD	Command MMC2	bidir
88	MMC2_DATA0	MMC2 dataline 0	Bidir
90	MMC2_DATA1	MMC2 dataline 1	Bidir
92	GND	Ground	Power
94	MMC2_DATA2	MMC2 dataline 2	Bidir
96	MMC2_DATA3	MMC2 dataline 3	Bidir
98	MMC2_DATA4	MMC2 dataline 4	Bidir
100	MMC2_DATA5	MMC2_dataline 5	Bidir
102	GND	Ground	Power
104	MMC2_DATA6	MMC2 dataline 6	bidir
106	MMC2_DATA7	MMC2 dataline 7	bidir
108	MMC1_DATA0	MMC1 dataline 0	bidir
110	MMC1_DATA1	MMC1 dataline 1	bidir
112	GND	Ground	Power
114	MMC1_DATA3	MMC1 dataline 3	bidir
116	SCH_TDO	TDO from SCH	Output
118	SCH_TDI	TDI from SCH	input
120	SCH_TCK	TCK from SCH	input
122	GND	Ground	Power
124	SCH_TMS	TMS from SCH	input
126	SCH_TRST	TRST from SCH	input
128	XDP_TDI	TDI from CPU	input
130	XDP_TDO	TDO from CPU	output
132	XDP_TMS	TMS from CPU	input
134	VCC1V05S (Refernce)	JTAG reference voltage for SCH and CPU	output
136	#USB_OC_5	Over current USB port 5	input
138	GND	Ground	Power
140	USB_DP_5	USB Port 5 pos. Dataline	Diff bidir
142	USB_DN_5	USB Port 5 neg. Dataline	Diff bidir
144	#USB_OC_4	Over current USB port 4	input
146	USB_DP_4	USB Port 4 pos. Dataline	Diff bidir
148	USB_DN_4	USB Port 4 neg. Dataline	Diff bidir
150	GND	Ground	Power
152	USB_DP_1	USB Port 1 pos. Dataline	Diff bidir

154	USB_DN_1	USB Port 1 neg. Dataline	Diff bidir
156	#USB_OC_1	Over current USB port 1	input
158	LA_CLKP	LVDS pos. clockline	Diff output
160	LA_CLKM	LVDS neg. clockline	Diff output
162	GND	Ground	Power
164	L_VDDEN	Enable for LCD power	output
166	L_CLKCTLA	LCD management Bus ClockA	
168	L_CLKCTLB	LCD management Bus ClockB	
170	L_DDC_DATA	DDC data	Bidir (PU)
172	LA_DATAP_2	LVDS data group 2 pos. signal	Diff output
174	LA_DATAM_2	LVDS data group 2 neg. signal	Diff output
176	GND	Ground	Power
178	SDVO_INT	SDVO INT pos. signal	
180	#SDVO_INT	SDVO INT neg. signal	
182	TP8	Future use	nc
184	L_BKLTCTL	LCD Backlight control	output
186	SDVOB_CLK	SDVOB Clock pos. signal	
188	#SDVOB_CLK	SDVOB Clock neg. signal	
190	GND	Ground	Power
192	SDVO_CTRLDATA	SDVO management data	Bidir (PU)
194	SDVOB_RED	SDVOB Red pos. signal	
196	#SDVOB_RED	SDVOB Red neg. signal	
198	GND	Ground	Power
200	SDVOB_BLUE	SDVOB blue pos. signal	
202	#SDVOB_BLUE	SDVOB blue neg. signal	
204	CSEL	Select between SSD/SATA Master/Slave	input
206	SDVOB_GREEN	SDVOB green pos. signal	
208	#SDVOB_GREEN	SDVOB green neg. signal	
210	GND	Ground	Power
212	CLK_PCIE_SLOT1	PCIe pos. clock for Slot 1	Diff output
214	#CLK_PCIE_SLOT1	PCIe neg. clock for Slot 1	Diff output
216	LAN_LED2	Ethernet Speed Led	Output (OD)
218	PCIE_TXP_2	Second PCIe Transmit pos.	Diff output
220	PCIE_TXN_2	Second PCIe Transmit neg.	Diff output
222	GND	Ground	Power
224	PCIE_RXP_2	Second PCIe receive pos.	Diff input
226	#PCIE_RXP_2	Second PCIe receive neg.	Diff input

228	#CLK_SLOT1_OE	Output enable for Slot 1 clock	Input (PU)
230	GND	Ground	Power
232	#SATA_RX	SATA receive neg. signal	Diff input
234	SATA_RX	SATA receive pos. Signal	Diff input
236	#DASP	SSD/SATA activity signal	output
238	SATA_TX	SATA transmit pos. signal	Diff output
240	#SATA_TX	SATA transmit neg. signal	Diff output

3 Jumpers

For configuration purposes, the phyCORE-Z500PT has 4 solder jumpers, some of which have been installed prior to delivery. *Figure 4* illustrates the numbering of the solder jumper pads, while *Figure 5* and *Figure 6* indicate the location of the solder jumpers on the board. Three solder jumpers are located on the top side of the module (opposite side of connectors). *Table 2* below provides a functional summary of the solder jumpers, their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable section listed in the table.

Figure 4: Numbering of the Jumper Pads

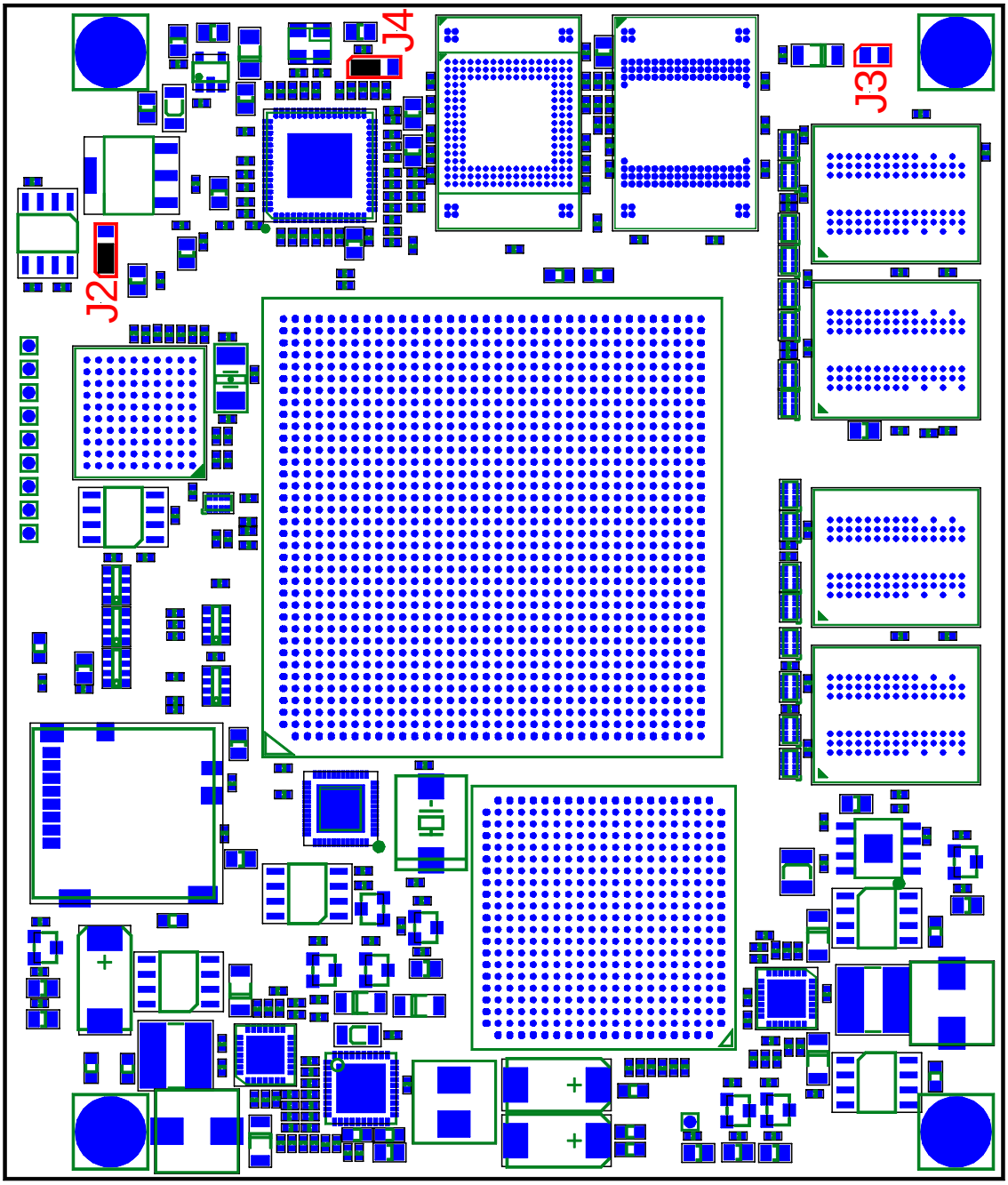


Figure 5: Location of the Jumpers (Top View)

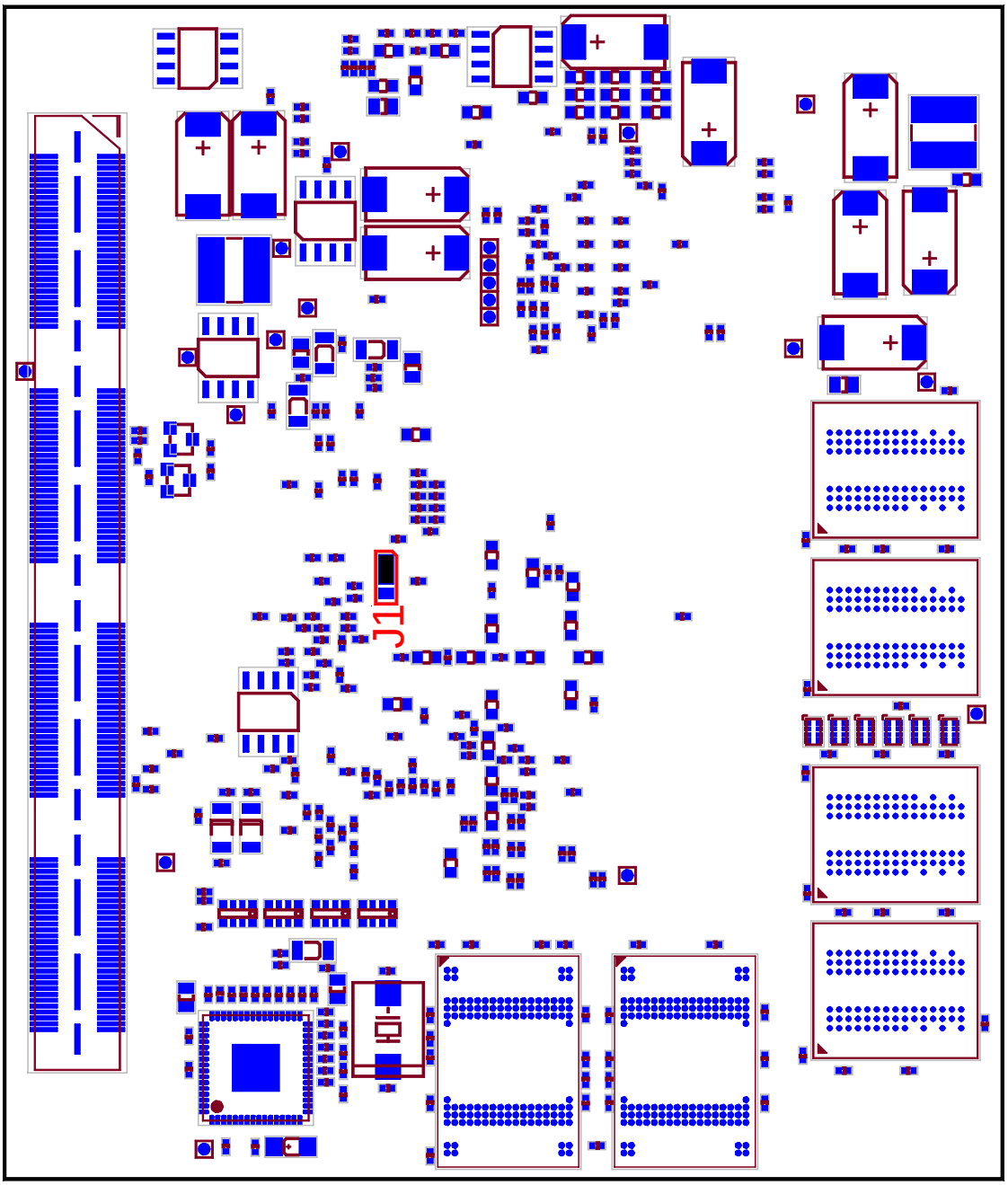


Figure 6: Location of the Jumpers (Bottom View)

The jumpers (J = solder jumper) have the following functions:

Table 2: Jumper Settings

	Default Setting		Alternative Setting		See Section
J1	1 + 2	Selects 3.3 V as I/O-Voltage for Intel® HDA audio interface.	1 + 3	Selects 1.5 V as I/O-Voltage for Intel® HDA audio interface.	
J2	1 + 2	The Ethernet controller is powered off during suspend.	1 + 3	The Ethernet controller is powered on during suspend.	
J3	open	Solid-State-Disk (SSD) is not write protected.	closed	Solid-State-Disk is write protected.	
J4	1 + 2	A SPI-Flash is used as configuration-/ROM-device for the Ethernet controller.	1 + 3	A SPI-EEPROM is used as configuration-/ROM-device for the Ethernet controller.	6.11.2

4 Power Requirements

The phyCORE-Z500PT normally operates off a single voltage supply denoted as VCC5VA.

Table 3: Power supply

power supply	min.	typ.	max.
5 V (VCC5VA)	4.5 V	5 V	5.5 V

The input voltage range of VCC5VA is from 4.5 V.. 5.5 V allowing a current draw of typically 700 mA.

See *Table 1* from *section 2* above for applicable VCC5VA power pins on the phyCORE-connector.

Caution!
Connect all VCC5VA input pins to your power supplies.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry.

5 CPU Intel® Z5xx (U1)

The phyCORE-Z500WP(T) can be populated with Intel® Atom Z510P/PT, Z520PT or Z530P microprocessor (packaging 437-ball, µFCBGA8 22 x 22 mm).
This results in different FSB/DDR2 frequencies and therefore different populated configuration resistors.

The following table shows the dependencies.

CPU at U1	Ordering Code / Marking	Temp. Range	FSB / DDR2	R247	R248	R249	R250
Z510P	CH80566EE005DW	0 – 70°C	400MHz	populated	-	-	populated
Z510PT	CH80566EE005DT	-40 – 85°C	400MHz	populated	-	-	populated
Z520PT	CH80566EE014DT	-40 – 85°C	533MHz	populated	-	populated	-
Z530P	CH80566EE025DW	0 – 70°C	533MHz	populated	-	populated	-

For more information take a look at

http://www.Intel® .com/design/intarch/atom500/index.htm

6 SCH US15WP(T) (U2)

The System Controller Hub (SCH) integrates a graphics memory controller hub and an I/O controller hub into one package.
The SCH provide all I/O like LPC Bus, LVDS, SDVO, SDIO/MMC, PCIe, USB, PATA, HDAudio GPIOs, JTAG and also the DDR2-Controller, which are described on the following pages.

SCH at U2	Ordering Code / Marking	Temp. Range	FSB / DDR2	GFX frequency	R247	R248
US15WP	LE82US15EC	0 – 70°C	400MHz/533MHz	200 MHZ	populated	-
US15WPT	LE82US15EE	-40 – 85°C	400MHz/533MHz	200 MHZ	populated	-

For more information take a look at

http://www.intel.com/design/intarch/atom500/index.htm

6.1 LPC Bus

The LPC Bus implemented in the SCH is used to connect Super-I/O controllers, Firmware-Hubs and other low speed peripheral to the phyCORE-Z500.
The LPC bus was specified from Intel® and the specification can be downloaded from

http://www.intel.com/design/chipsets/industry/lpc.htm

Signal-Name	Description	Nr. @ X2	on board circuit	Type	Remark
CLK_LPC_PORT80	LPC Clock used for Port 80	**39**	SR 20 Ohm	O CMOS3.3	
CLK_LPC_TPM	LPC Clock for TPM	**40**	SR 20 Ohm	O CMOS3.3	
CLK_LPC_FWH	LPC Clock for FWH	**43**	SR 20 Ohm	O CMOS3.3	Used on board for FWH
LPC_FRAME	LPC Frame Signal	**45**		O CMOS3.3	
#LPC_CLKRUN	LPC Clock Gate	**47**	PU 10k Ohm	I/O CMOS3.3	
LPC_SERIRQ	LPC interrupt line	**49**	PU 10k Ohm	I/O CMOS3.3	
LPC_AD0	LPC Bus Address 0	**44**	IPU 50k Ohm	I/O CMOS3.3	
LPC_AD1	LPC Bus Address 1	**46**	IPU 50k Ohm	I/O CMOS3.3	
LPC_AD2	LPC Bus Address 2	**48**	IPU 50k Ohm	I/O CMOS3.3	
LPC_AD3	LPC Bus Address 3	**50**	IPU 50k Ohm	I/O CMOS3.3	

Table 4: LPC-Bus signals

6.2 LVDS Interface

The Intel® SCH supports a Low-Voltage Differential Signaling interface that allows the Intel® Graphics Media Adapter to communicate directly to an flat-panel display. The LVDS interface supports pixel color depths of 18-and 24-bits.

Signal-Name	Description	Nr. @ X2	on-board circuit	Type	Trace length on phyCORE	Remark
LA_CLKP	LVDS pos. clockline	158	IPU 50 Ohm	O LVDS	48 mm	
LA_CLKM	LVDS neg. clockline	160	IPU 50 Ohm	O LVDS		
LA_DATAP_0	LVDS data group 0 pos. signal	165	IPU 50 Ohm	O LVDS	58 mm	
LA_DATAM_0	LVDS data group 0 neg. signal	167	IPU 50 Ohm	O LVDS		
LA_DATAP_1	LVDS data group 1 pos. signal	171	IPU 50 Ohm	O LVDS	60 mm	
LA_DATAM_1	LVDS data group 1 neg. signal	173	IPU 50 Ohm	O LVDS		
LA_DATAP_2	LVDS data group 2 pos. signal	172	IPU 50 Ohm	O LVDS	46 mm	
LA_DATAM_2	LVDS data group 2 neg. signal	174	IPU 50 Ohm	O LVDS		
LA_DATAP_3	LVDS data group 3 pos. signal	177	IPU 50 Ohm	O LVDS	50 mm	
LA_DATAM_3	LVDS data group 3 neg. signal	179	IPU 50 Ohm	O LVDS		
L_BKLTCTL	LCD Backlight control	184		O CMOS3.3		
L_BKLTEN	LCD Backlight enable	183	PD 100k Ohm	O CMOS3.3		
#L_BKLTSEL_0_GPIO	LVDS Backlight select / GPIO	54		I/O CMOS3.3		Could be used as GPIO
#L_BKLTSEL	LVDS Backlight select / GPIO	68		O CMOS3.3		Could be used as GPIO
L_VDDEN	Enable for LCD power	164	PD 100k Ohm	O CMOS3.3		
L_CLKCTLA	LCD management Bus ClockA	166	PU 4.7k Ohm	I/O CMOS3.3_OD		
L_CLKCTLB	LCD management Bus ClockB	168	**PU 4.7k Ohm**	I/O CMOS3.3_OD		PU missing on PCB1310.1
L_DDC_DATA	DDC data	170	PU 10k Ohm	I/O CMOS3.3_OD		
L_DDC_CLK	DDC clock	169	PU 10k Ohm	I/O CMOS3.3_OD		

Table 5: LVDS-Signals

According to the Intel® Design guide, the LVDS clock- an data- signals should be length-matched to within ±0.508 mm (±20 mils). The maximum recommended trace length from the SCH to the LVDS connector is 170 mm including the on die package length. Also the LVDS cable should have an impedance of 97 Ohm ± 20 % and a maximum length of 177,8 mm (7 inches).

6.3 SDIO/MMC Interface

The Intel® SCH has three integrated SDIO/MMC interfaces, all of them are available at connector X2. Port 0 is equipped at the phyCORE-Z500WP(T) and accessible at X1. The LED D10 beside the micro-SD holder shows if there is activity.
Port 0 and port 1 are 4 bit wide while port 2 is 8 bits wide. If port 0 should be used on the customer board, it should not populated on the phyCORE-Z500WP(T).

Signal-Name	Description	Nr. @ X2	on -board circuit	Type	Trace length on phyCORE	Remark
MMC_0_LED	Activity output MMC0	73		O CMOS3.3	55 mm	used on the phyCORE-Z500WP(T) at MMC/SDIO socket X1
#MMC0_CD	Card detect MMC0	75	PU 10k Ohm	I CMOS3.3		
MMC0_WP	Write protect MMC0	77	PU 10k Ohm	I CMOS3.3		
#MMC0_PWR	Power enable output MMC0	79	IPU 60k Ohm SR 47 Ohm	O CMOS3.3		
MMC0_CLK	Clock MMC0	83	SR 47 Ohm	O CMOS3.3		
MMC0_CMD	Command MMC0	85	PU 10k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC0_DATA0	MMC0 dataline 0	87	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC0_DATA1	MMC0 dataline 1	89	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC0_DATA2	MMC0 dataline 2	93	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC0_DATA3	MMC0 dataline 3	95	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC1_LED	Activity output MMC1	97		O CMOS3.3		
#MMC1_CD	Card detect MMC1	99	PU 10k Ohm	I CMOS3.3		
MMC1_WP	Write protect MMC1	103	PU 10k Ohm	I CMOS3.3		
#MMC1_PWR	Power enable output MMC1	105	IPU 60k Ohm SR 47 Ohm	O CMOS3.3		
MMC1_CMD	Command MMC1	107	SR 47 Ohm	O CMOS3.3	45 mm	
MMC1_CLK	Clock MMC1	109	PU 10k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC1_DATA0	MMC1 dataline 0	108	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC1_DATA1	MMC1 dataline 1	110	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC1_DATA2	MMC1 dataline 2	113	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC1_DATA3	MMC1 dataline 3	114	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC_2_LED	Activity output MMC2	74		O CMOS3.3		
#MMC2_CD	Card detect MCM2	76	PU 10k Ohm	I CMOS3.3		
MMC2_WP	Write protect MMC2	78	PU 10k Ohm	I CMOS3.3		
#MMC2_PWR	Power enable output MMC2	80	IPU 60k Ohm SR 47 Ohm	O CMOS3.3		
MMC2_CLK	Clock MMC2	84	SR 47 Ohm	O CMOS3.3	55mm	
MMC2_CMD	Command MMC2	86	PU 10k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC2_DATA0	MMC2 dataline 0	88	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		

MMC2_DATA1	MMC2 dataline 1	90	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC2_DATA2	MMC2 dataline 2	94	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC2_DATA3	MMC2 dataline 3	96	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC2_DATA4	MMC2 dataline 4	98	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC2_DATA5	MMC2_dataline 5	100	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC2_DATA6	MMC2 dataline 6	104	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		
MMC2_DATA7	MMC2 dataline 7	106	IPU 75k Ohm SR 47 Ohm	I/O CMOS3.3		

According to the Intel® Design guide, the maximum recommended trace length from the SCH to the MMC/SDIO connector should be less or equal 127 mm (5000 mils).

6.4 SDVO

The Intel® SCH has a digital display channel capable of driving SDVO adapters that provide interfaces to a variety of external display technologies (e.g., DVI, TV-Out, analog CRT).

Signal-Name	Description	Nr. @ X2	On-board circuit	Type	Trace length on phyCORE	Remark
SDVO_TVCLKIN	SDVO TVCLKIN pos. signal	**185**	IPU 50 Ohm SC 100nF	O LVDS		
#SDVO_TVCLKIN	SDVO TVCLKIN neg. signal	**187**	IPU 50 Ohm SC 100nF	O LVDS		
SDVO_CTRLDATA	SDVO management data	**192**	PU 10k Ohm	I/O CMOS3.3		
SDVO_CTRLCLK	SDVO management clock	**191**	PU 10k Ohm	I/O CMOS3.3		
SDVOB_CLK	SDVOB Clock pos. signal	**186**	IPU 50 Ohm SC 100nF	O LVDS		
#SDVOB_CLK	SDVOB Clock neg. signal	**188**	IPU 50 Ohm SC 100nF	O LVDS		
SDVO_INT	SDVO INT pos. signal	**178**	IPU 50 Ohm SC 100nF	O LVDS		
#SDVO_INT	SDVO INT neg. signal	**180**	IPU 50 Ohm SC 100nF	O LVDS		
SDVOB_STALL	SDVOB STALL pos. signal	**193**	IPU 50 Ohm SC 100nF	O LVDS		
#SDVOB_STALL	SDVOB STALL neg. signal	**195**	IPU 50 Ohm SC 100nF	O LVDS		
SDVOB_RED	SDVOB Red pos. signal	**194**	IPU 50 Ohm SC 100nF	O LVDS		
#SDVOB_RED	SDVOB Red neg. signal	**196**	IPU 50 Ohm SC 100nF	O LVDS		
SDVOB_GREEN	SDVOB green pos. signal	**206**	IPU 50 Ohm SC 100nF	O LVDS		
#SDVOB_GREEN	SDVOB green neg. signal	**208**	IPU 50 Ohm SC 100nF	O LVDS		
SDVOB_BLUE	SDVOB blue pos. signal	**200**	IPU 50 Ohm SC 100nF	O LVDS		
#SDVOB_BLUE	SDVOB blue neg. signal	**202**	IPU 50 Ohm SC 100nF	O LVDS		

6.5 PCIe

On the pyhCORE-Z500P(Z) are two PCIe x 1 lanes available. The first on is connected to the on-board Intel® GB-Ethernet controller 82574I. The second PCIe lane is directly connected to the connector X2. Both PCIe lanes are supplied wit a separate clock from the clock-generator U26 and have separate clock enable signals.
If the on-board Ethernet controller is not populated, also the first PCIe lane can be accessed at X2.

Signal-Name	Description	Nr. @ X2	on-board circuit	Type	Trace length on phyCORE	Remark
#PCIE_WAKE	Wake Signal	**227**		I CMOS3.3 PU 1k Ohm		
#CLK_SLOT0_OE	Output enable for Slot 0 clock	**235**		I CMOS3.3 IPU 10k Ohm		
CLK_PCIE_SLOT0_CON	PCIe pos. clock for Slot 0	**223**		O LVDS ISR 33Ohm		
#CLK_PCIE_SLOT0_CON	PCIe neg. clock for Slot 0	**225**		O LVDS ISR 33Ohm		
PCIE_TXP_1_CON	First PCIe Transmit pos.	**231**	SC 100nF	O PCIe		
#PCIE_TXN_1_CON	First PCIe Transmit neg.	**233**	SC 100nF	O PCIe		
PCIE_RXP_1_CON	First PCIe receive pos.	**237**		I PCIe		
PCIE_RXN_1_CON	First PCIe receive neg.	**239**		I PCIe		
#CLK_SLOT1_OE	Output enable for Slot 1 clock	**228**		I CMOS3.3 IPU 10k Ohm		
CLK_PCIE_SLOT1	PCIe pos. clock for Slot 1	**212**		O LVDS ISR 33Ohm		
#CLK_PCIE_SLOT1	PCIe neg. clock for Slot 1	**214**		O LVDS ISR 33Ohm		
PCIE_TXP_2	Second PCIe Transmit pos.	**218**	SC 100nF	O PCIe		
PCIE_TXN_2	Second PCIe Transmit neg.	**220**	SC 100nF	O PCIe		
PCIE_RXP_2	Second PCIe receive pos.	**224**		I PCIe		
#PCIE_RXP_2	Second PCIe receive neg.	**226**		I PCIe		

6.5.1 Ethernet Controller Intel® 82574I (U16)

Connection of the phyCORE-Z500P(T) to the world wide web (WWW) or a local area network (LAN) is possible with the Intel® 82574I (U16) 10/100/1000 Mbps Ethernet controller with HP Auto-MDIX populating the module at U16. This Ethernet controller features an integrated PHY layer.
Thus the external components required to connect the phyCORE-Z500P(T) to a LAN are limited to the transformer, the RJ45 socket and a few discrete components. Support for this Ethernet chip is available by a wide range of operating systems, such as Linux and WinXP.

The Ethernet controller is connected to the first PCIe x 1 lane. If the controller is not populated, the first PCIe x 1 lane is also available at X2.

Connection to an external Ethernet transformer should be done using very short signal lines. The lines MDI_PLUS[1..3] and MDI_MINUS[1..3] should be routed in pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals. Furthermore, the impedance of the signal lines should be taken into consideration during the design and layout process.

Signal-Name	Description	Nr. @ X2	on-board circuit	Type	Remark
MDI_PLUS0	MDI0 pos. signal	199		I/O DIFF	
MDI_MINUS0	MDI0 neg. signal	201		I/O DIFF	
MDI_PLUS1	MDI1 pos. signal	205		I/O DIFF	
MDI_MINUS1	MDI1 neg. signal	207		I/O DIFF	
MDI_PLUS2	MDI2 pos. signal	211		I/O DIFF	
MDI_MINUS2	MDI2 neg. signal	213		I/O DIFF	
MDI_PLUS3	MDI3 pos. signal	217		I/O DIFF	
MDI_MINUS3	MDI3 neg. signal	219		I/O DIFF	
LAN_LED0	Activity Led	203		O CMOS3.3	±12 mA
LAN_LED1	Link Led	215		O CMOS3.3	±12 mA
LAN_LED2	Speed Led	216		O CMOS3.3	±12 mA

Caution!
Please note the design specifications provided by Intel® when creating the Ethernet transformer circuitry.

6.6 USB

The Intel® SCH provides eight USB ports with high-speed transfer rates up to 480 Mb/s. Port 2 can be used as USB-Client together with SCH_GPIOUS3 as indicator for a connection with an USB host. Port 6 and 7 should only be used for in-system USB2.0 devices.
All ports are available at the connector X2.

Signal-Name	Description	Nr. @ X2	on-board circuit	Type	Trace length on phyCORE	Remark
SCH_GPIOUS_3	USB Client connect	**56**	PD 100k Ohm	I/O CMOS3.3		If USB Port2 is used for client mode.
#USB_OC_7	Over current USB port 7	**129**	PU 10k Ohm	I CMOS3.3		
USB_DP_7	USB Port 7 pos. Dataline	**131**		I/O USB IPD 15k Ohm		EHCI only
USB_DN_7	USB Port 7 neg. Dataline	**133**		I/O USB IPD 15k Ohm		EHCI only
#USB_OC_6	Over current USB port 6	**135**	PU 10k Ohm	I CMOS3.3		
USB_DP_6	USB Port 6 pos. Dataline	**139**		I/O USB IPD 15k Ohm		EHCI only
USB_DN_6	USB Port 6 neg. Dataline	**141**		I/O USB IPD 15k Ohm		EHCI only
#USB_OC_3	Over current USB port 3	**143**	PU 10k Ohm	I CMOS3.3		
USB_DP_3	USB Port 3 pos. Dataline	**145**		I/O USB		
USB_DN_3	USB Port 3 neg. Dataline	**147**		I/O USB		
USB_DP_2	USB Port 2 pos. Dataline	**151**		I/O USB IPD 15k Ohm		IPU 1.5k Ohm (client mode)
USB_DN_2	USB Port 2 neg. Dataline	**153**		I/O USB IPD 15k Ohm		IPU 1.5k Ohm (client mode)
#USB_OC_2	Over current USB port 2	**155**	PU 10k Ohm	I CMOS3.3		
USB_DP_0	USB Port 0 pos. Dataline	**157**		I/O USB IPD 15k Ohm		
USB_DN_0	USB Port 0 neg. Dataline	**159**		I/O USB IPD 15k Ohm		
#USB_OC_0	Over current USB port 0	**163**	PU 10k Ohm	I CMOS3.3		
#USB_OC_5	Over current USB port 5	**136**	PU 10k Ohm	I CMOS3.3		
USB_DP_5	USB Port 5 pos. Dataline	**140**		I/O USB IPD 15k Ohm		
USB_DN_5	USB Port 5 neg. Dataline	**142**		I/O USB IPD 15k Ohm		
#USB_OC_4	Over current USB port 4	**144**	PU 10k Ohm	I CMOS3.3		
USB_DP_4	USB Port 4 pos. Dataline	**146**		I/O USB IPD 15k Ohm		
USB_DN_4	USB Port 4 neg. Dataline	**148**		I/O USB IPD 15k Ohm		
USB_DP_1	USB Port 1 pos. Dataline	**152**		I/O USB IPD 15k Ohm		
USB_DN_1	USB Port 1 neg. Dataline	**154**		I/O USB IPD 15k Ohm		
#USB_OC_1	Over current USB port 1	**156**	PU 10k Ohm	I CMOS3.3		

6.7 PATA/IDE

The Intel® SCH provides an PATA-Interface which is able to drive an IDE Master-/Slave configuration. It support PIO, ATA-5 (66 MB/s) and Ultra-DMA (33/66/100). A transfer rate up to 100 MB/s is supported.
At the phyCORE-Z500P(T) the PATA interface is used to connect a Solid State Disk and a SATA-II bridge. Both can be Master or Slave. This is controlled by the CSEL signal which is routed to X2.
SDD/SATA activity can be monitored via the #DASP signal.

Signal-Name	Description	Nr. @ X2	on-board circuit	Type	Remark
CSEL	Select between SSD/SATA Master/Slave	204	PU 10k Ohm	I CMOS3.3	
#DASP	SSD/SATA activity signal	236	PU 475 Ohm, LED	O CMOS3.3	

CSEL	SSD	SATA-II Bridge
0 (GND)	Slave	Master
1 (3.3V)	Master	Slave

6.7.1 Solid State Disk SSD (U4,U5,U6,U7)

It is possible to populate 2/4/8/16 GByte SSD on the phyCORE-Z500P(T). Therefore the ntel® Z-P140 PATA SSD with 2 Gbyte or 4 GByte are used. The following table shows which of the devices are populated for the different sizes.

2 Gbyte devices (SSDPAPS0002G1)

SSD size	U4	U5	U6	U7
2Gbyte	SSDPAPS0002G1	---	---	---
4Gbyte	SSDPAPS0002G1	---	PF29F16G32PANC1	---
8Gbyte	SSDPAPS0002G1	PF29F16G32PANC1	PF29F16G32PANC1	PF29F16G32PANC1

4 Gbyte devices (SSDPAPS0004G1)

SSD size	U4	U5	U6	U7
4Gbyte	SSDPAPS0004G1	---	---	---
8Gbyte	SSDPAPS0004G1	---	PF29F32G32PANC1	---
16Gbyte	SSDPAPS0004G1	PF29F32G32PANC1	PF29F32G32PANC1	PF29F32G32PANC1

Caution!
This feature is subject to change. Intel® has discontinued these parts. Phytec will provide a solution or updated version of the current PCB. It is intended that this new solution will not impact any current designs.
Please contact our support-/sales-team for further information.

6.7.2 SATA-II Bridge 88SA8052 (U19)

The Marvell SATA-II Bridge 88SA8052 is used to make it possible to expand the available mass storage memory with standard SATA hard disks.

Signal-Name	Description	Nr. @ X2	on-board circuit	Type	Trace length on phyCORE	Remark
#SATA_RX	SATA receive neg. signal	232	SC 10nF	I SATA		100Ohm diff., 50 Ohm char.
SATA_RX	SATA receive pos. Signal	234	SC 10nF	I SATA		100Ohm diff., 50 Ohm char.
SATA_TX	SATA transmit pos. signal	238	SC 10nF	O SATA		100Ohm diff., 50 Ohm char.
#SATA_TX	SATA transmit neg. signal	240	SC 10nF	O SATA		100Ohm diff., 50 Ohm char.

6.8 Intel® High Definition Audio (Intel® HD Audio)

The Intel® SCH provides an interface for different Intel® High Definition Audio/modem codes. All the signals are available at X2. For further information regarding the Intel® High Definition Audio Secification visit

http://www.intel.com/standards/hdaudio/index.htm

Signal-Name	Description	Nr. @ X2	on-oard circuit	Type	Trace length on phyCORE	Remark
HDA_SDI_0	Intel® HD Audio Serial Data in	13		I CMOS HDA IPD 22k Ohm		
HDA_SDI_1	Intel® HD Audio Serial Data in	15		I CMOS HDA IPD 22k Ohm		
#HDA_DOCKEN	Intel® HD Dock Enable	17		O CMOS HDA		
#HDA_DOCKRST	Intel® HD Dock Reset	19		O CMOS HDA IPD 20k Ohm		
HDA_RST	Intel® HD Audio Reset	21	SR 33Ohm	O CMOS HDA IPD 22k Ohm		
HDA_CLK	Intel® HD Audio Clock	16	SR 33Ohm	O CMOS HDA IPD 22k Ohm		
HDA_SDO	Intel® HD Audio Serial Data Out	18	SR 33Ohm	O CMOS HDA IPD 22k Ohm		
HDA_SYNC	Intel® HD Audio Sync	20	SR 33Ohm	O CMOS HDA IPD 22k Ohm		

6.9 GPIOs

The Intel® SCH contains a total of 14 GPIO pins. Ten GPIOs are powered by the core power rail and are turned off during sleep modes (S3 and higher). The remaining four GPIOs are powered by the system controller hub suspend well power supply. These GPIOs and remain active during S3. The suspend well GPIOs can be used to wake the system from the Suspend-to-RAM state.
The GPIOs are not 5 V tolerant.

Signal-Name	Description	Nr. @ X2	on-board circuit	Type	Trace length on phyCORE	Remark
GPIO_SUS0		53	PD 10k Ohm			
#L_BKLTSEL_0_GPIO (GPIO_SUS1)		54				
#PM_PWRBTTN (GPIO_SUS2)	Debounced copy of #SMC_ONOFF	55				Used for System Managment
SCH_GPIOSUS_3		56	PD 100k Ohm			
GPIO_0		57	PD 10k Ohm	IPD 22k Ohm		
GPIO_1		58	PD 10k Ohm			
GPIO_2		59	PU 10k Ohm			
GPIO_3		60	PU 10k Ohm	IPU 22k Ohm		
GPIO_4		63				
GPIO_5		64				
GPIO_6		65	PU 10k Ohm			
#SLPIOVR (GPIO_7)		66				Used for System Managment
GPIO_8		67	PU 10k Ohm			Used for System Managment
#L_BKLTSEL (GPIO_9)		68				

6.10 JTAG

There are three devices on the phyCORE-Z500P(T) where JTAG can be used to do a boundary scan or reprogram the device. These devices are the Z500P(T), the SCH and the Altera EPM240/570.

Signal-Name	Description	Nr. @ X2	on-board circuit	Type	Remark
PLD_TDO	TDO from PLD	115		O CMOS3.3	
PLD_TDI	TDI from PLD	117	PU 10k Ohm	I CMOS3.3	
PLD_TCK	TCK from PLD	119	PD 10k Ohm	I CMOS3.3	
PLD_TMS	TMS from PLD	123	PU 10k Ohm	I CMOS3.3	
XDP_TRST	TRST from CPU	125	PD 56 Ohm	I CMOS1.05	
XDP_TCK_0	TCK from CPU	127	PD 56 Ohm	I CMOS1.05	
XDP_TDI	TDI from CPU	128	PU 56 Ohm	I CMOS1.05	
XDP_TDO	TDO from CPU	130	PU 56 Ohm	O CMOS1.05	
XDP_TMS	TMS from CPU	132	PD 56 Ohm	I CMOS1.05	
SCH_TDO	TDO from SCH	116	PU 56 Ohm	OD CMOS1.05	
SCH_TDI	TDI from SCH	118	PU 56 Ohm	IPU 5k Ohm I CMOS1.05	
SCH_TCK	TCK from SCH	120	PU/PD 56 Ohm	IPU 5k Ohm I CMOS1.05	
SCH_TMS	TMS from SCH	124	PU 56 Ohm	IPU 5k Ohm I CMOS1.05	
SCH_TRST	TRST from SCH	126	PD 56 Ohm	IPU 5k Ohm I CMOS1.05	

6.11 SMB

The Intel® SCH provides an SMB interface which is used on board to connect an SPD-EEPROM (U3), the Clock-Generator (U26) and the management port of the 82574 Ethernet controller.

6.11.1 Clock-Generator (U26)

On the phyCORE-Z500P(T) a clock-generator from IDT is used to generate the different clock domains for i.e. PCIe Slot 0/1, PCIe core, CPU-BCLK, SCH-BCLK, Display-PLL A/B.
Both PCIe clocks can be separately enabled by driving CLK_SLOT1_OEn / CLK_SLOT2_OEn to GND.
The Clock-Generator is connected to the SMB bus and can be accessed with I²C address 0xD2.

6.11.2 I²C EEPROM (U3)

The phyCORE-Z500P(T) is populated with a Catalyst 24W32C[1] non-volatile 4 KByte EEPROM (U3) with an I²C interface to store BIOS configuration data and/or SPD data. This device is accessed through I²C with the address 0xA0.

6.12 DDR2-SDRAM Interface (U9-12,U8,U14,U13,U15)

The Intel® SCH support up to 2 GByte DDR2 memory on two ranks. Rank 1 include U9,10,11,12 at the top and Rank 2 include U8,U13,U14,U15 at the bottom side of the phyCORE-Z500P(T).

1: See the manufacturer's data sheet for interfacing and operation.

7 LPC to SPI Bridge / Power-Management (U21)

Due to the information that most manufactures of Firmware-Hub's (FWH) will discontinue the production of FWH with LPC interface, a LPC ⇔SPI bridge is used on the phyCORE-Z500P(T). This bridge is realized inside the Altera EPM570 PLD.
A second function of this PLD is Power-Management.

7.1 BIOS SPI-Flash (U17)

The SPI-Flash at U17 hold the BIOS for the phyCORE-Z500P(T). It is accessed via the LPC ⇔SPI bridge realized inside the Altera EPM570 PLD. U17 can be populated with many different SPI-Flash devices but only the following are supported at the moment.

Type	Manufacturer	Size
AT26DF081A	Atmel	1MByte
AT26DF160A	Atmel	2MByte

If a 2 MByte sized SPI-Flash is populated, the signal FWH_BSEL select between the upper/lower bank. With this, a "backup-BIOS" is still available in the other bank.

To reflash the BIOS the tool "spiprog" is used, which you can find on the CD.

The on-board BIOS can be disabled by pulling down the signal FWH_EN which has an 10kOhm pull-up at the phyCORE. This is useful to use a LPC-Flash as BIOS storage device.

Signal-Name	Description	Nr. @ X2	on-board circuit	Type	Remark
FWH_BSEL	BIOS bank select input	23		I CMOS3.3	
FWH_EN	disable on board FWH	25	PU 10k Ohm	I CMOS3.3	

8 Real Time Clock / CMOS Battery

The connection of a battery is not essential to the functioning of the phyCORE-Z500P(T). The battery, interfaced as voltage supply signal VBAT through X2 pin 14 on the phyCORE-connector, provides power to the CMOS and the internal Real Time Clock. This provides a means of time/BIOS-settings keeping in the absence of power at the VCC5VA pins while drawing minimal power from the battery.

The VBAT (2.0V < VBAT < 3.3V) input operating limits are listed in Table 6 below.

Table 6: VBAT Operating Limits

	MIN	TYP	MAX	UNITS
VBAT	2.0 V	3.3 V	3.6 V	V

If you choose not to use a battery with the phyCORE-Z500P(T) then VBAT should be not connected.

See section 9 Technical Specifications for battery power consumption.

9 Technical Specifications

The physical dimensions of the phyCORE-Z500P(T) are represented in *Figure 7*. The module's profile is approximately ***11.4 mm*** thick, with a maximum component height of ***5.0 mm*** on the bottom (connector) side of the PCB and approximately ***5.0 mm*** on the top (CPU/SCH) side. The board itself is approximately ***1.4 mm*** thick.

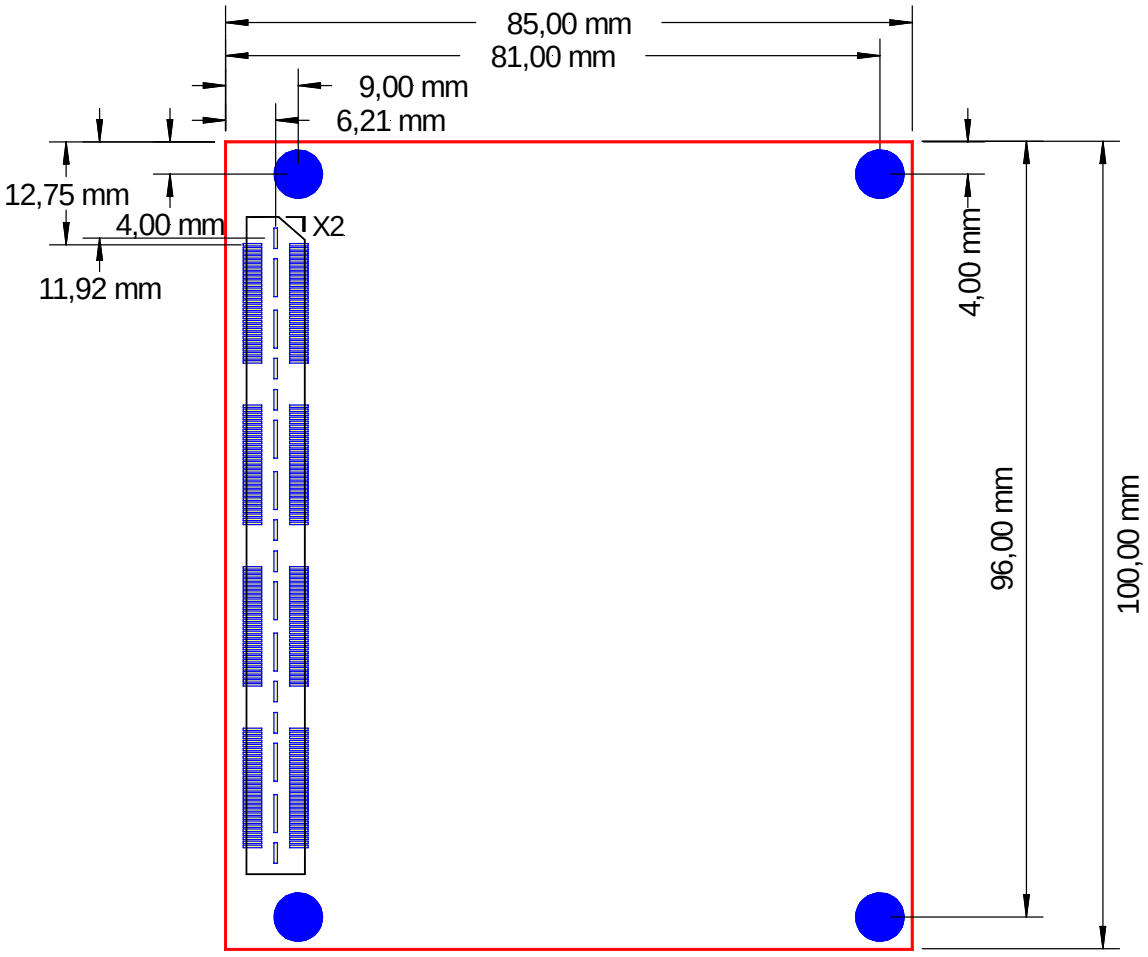


Figure 7: Physical Dimensions

Additional specifications:

• *Dimensions:*	*85 mm x 100 mm*
• *Weight:*	*approximately 57 g with all optional components mounted on the circuit board*
• *Storage temperature:*	*-40°C to +125°C*
• *Operating temperature:*	*0°C to +70°C (commercial)* *-45°C to +85°C (industrial)*
• *Humidity:*	*95 % r.F. not condensed*
• *Operating voltage:*	*VCC5VA 4.5 V to 5.5 V* *VBAT 2.0 to 3.6 V*
• *Power consumption:*	*Conditions:* ***VCC5VA = 5 V, VBAT = 3.3 V**,* *512 MByte DDR2-SDRAM, 2 GByte SSD, Ethernet, SATA, 1.1 GHz CPU frequency at 20°C* *Typ. 700 mA@5 V, max. 5 W*

These specifications describe the standard configuration of the phyCORE-Z500P(T) as of the printing of this manual.

10 Hints for Handling the phyCORE-Z500PT

Removal of various components, such as solder jumper and configuration resistors, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

11 The phyCORE Z500P(T) on the Carrier Board

PHYTEC Carrier Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Carrier Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

11.1 Connectors

Table 7 lists all available connectors on the phyCORE-Z500P(T) Carrier Board. *Figure 8: Carrier Board connector location"* highlights the location of each connector for easy identification.

Table 7: Carrier Board connectors

REFERENCE DESIGNATOR	DESCRIPTION
X1	Module connector, Samtec QTH-120-02-L-D-A
X4	JTAG-Port for PCIe Switch
X5	USB Port 3
X6	PCIe Slot 0
X7	PCIe Slot 1
X8	miniPCIe Slot 0
X9	SATA connector
X10	FPGA JTAG-Port
X11	HSMA JTAG-Port
X12	JTAG-Port for baseboard PLD
X14	RS232 header
X15	Header for front panel
X16	GPS external antenna connector
X17	Bluetooth external antenna connector
X18	Sim card holder
X19	Header for audio signals
X20	CD audio connector
X21	touch connector
X22	LPT printer
X23	RS232 (COM1)
X24	PS/2 keyboard/mouse
X25	DVI (only digital)
X26	miniUSB (OTG)
X27	Ethernet/2 x USB

X28	Audio
X29	LVDS display
X30	1-Wire
X31	MMC/SD Port 1
X32	MMC/SD Port 2
X33	HSMC connector
X34	JTAG-Port for CPU on phyCORE (XDP)
X35	JTAG-Port for SCH on phyCORE
X36	JTAG-Port for PLD on phyCORE
X37	Main Power-input 5V/3A

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user‘s responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

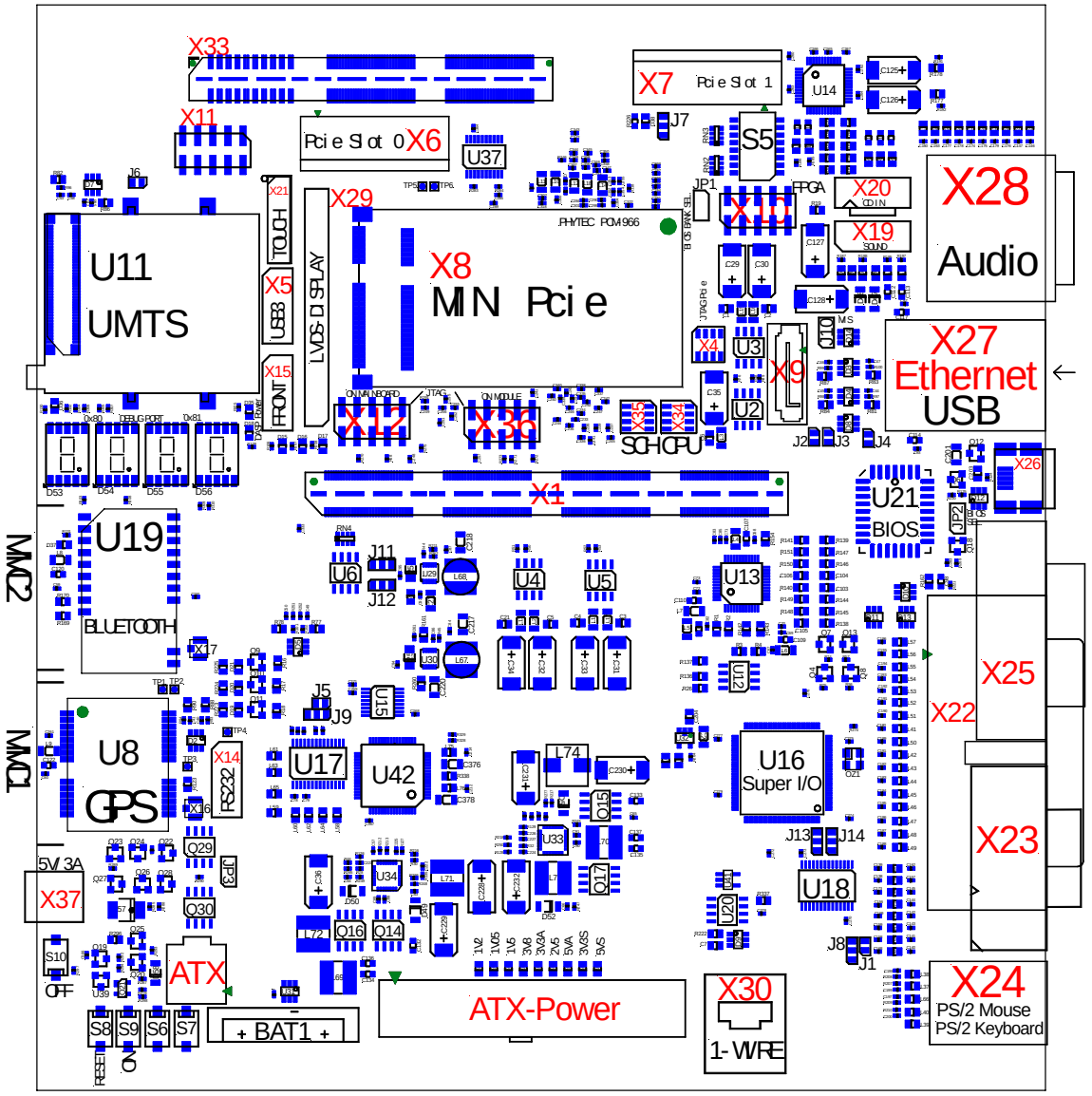


Figure 8: Carrier Board connector location top side

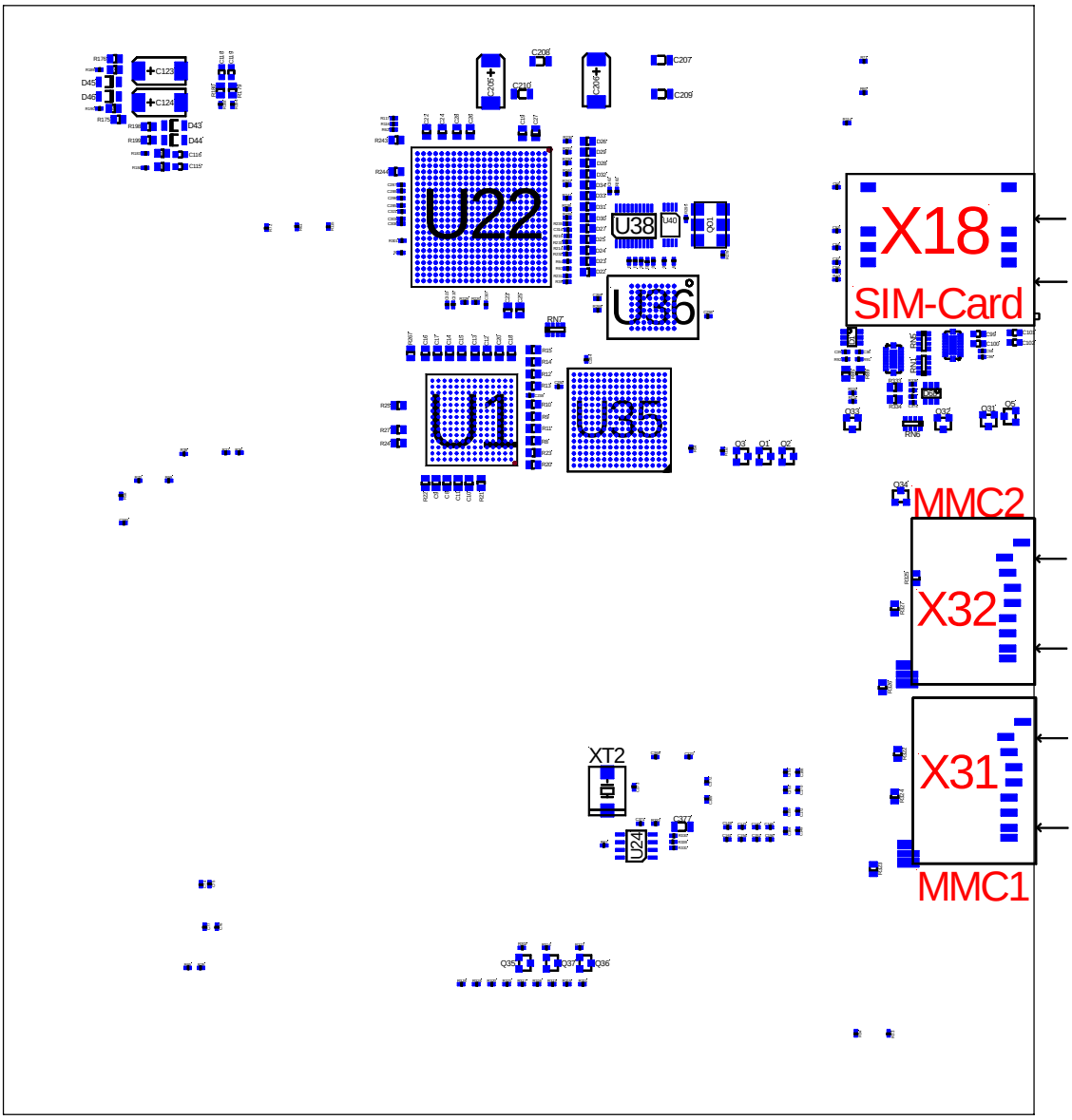


Figure 9: Carrier Board connector location bottom side

11.2 Jumpers on the Baseboard PCM-966

Carrier Board jumpers allow a variety of signal configurations and connectivity options between the phyCORE-Z500P(T) module and Carrier Board peripheral connectors. Before making connection to peripheral connectors it is a good idea to consult the applicable section in this manual for setting the associated jumpers.

See Table 8 for default settings and descriptions of all Carrier Board jumpers.

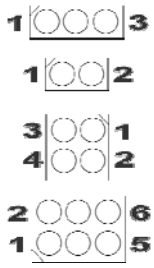


Figure 10: Typical jumper numbering scheme

Figure 10 illustrates the numbering scheme for various jumper blocks. Note that in each case pin 1 is always marked with a clipped corner on the PCB silk screen. *Figure 11* highlights the locations of all user configurable jumpers on the phyCORE-Z500P(T) Carrier Board.

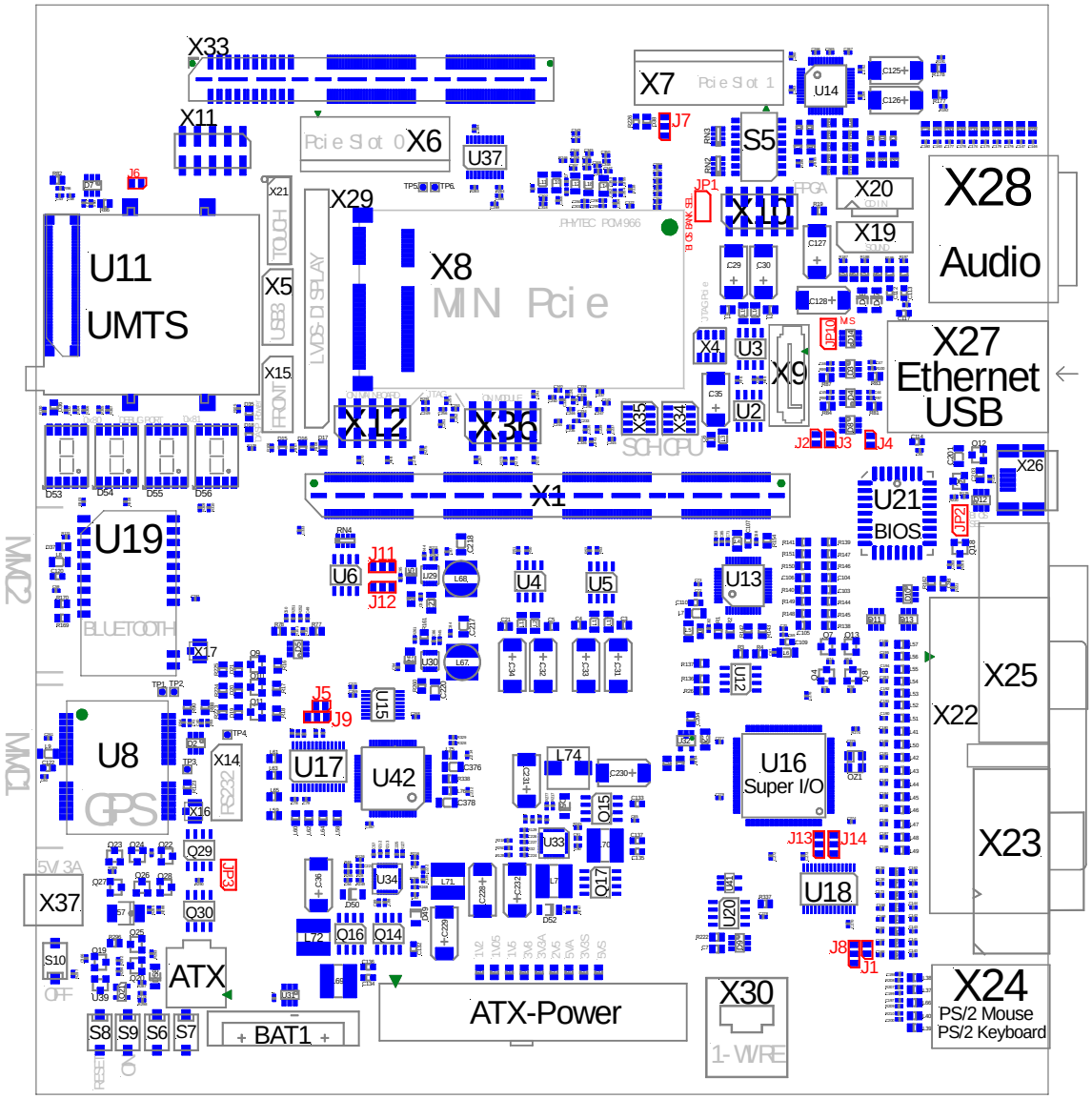


Figure 11: Carrier Board jumper location

Table 8: Carrier Board jumper descriptions[1]

JUMPER	SETTING	DESCRIPTION	SEE SECTION
JP1	**Open** Closed	**BIOS Bank 0 is selected** BIOS Bank 1 is selected (if available)	
JP2	Open **Closed**	BIOS on phyCORE-Z500P(T) is enabled **BIOS on phyCORE-Z500P(T) is disabled**	
JP3	**Open** Closed	**On-Board Power is switched by Power Management** On Board Power is forced on	
J10	**Open** closed	**SDD is Master / SATA is Slave** SATA is Master / SDD is Slave	

1 Default settings are in **bold blue** text

11.3 Functional Components on the phyCORE-Z500P(T) Carrier Board

This section describes the functional components of the phyCORE-Z500P(T) Carrier Board supporting the phyCORE-Z500P(T). Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

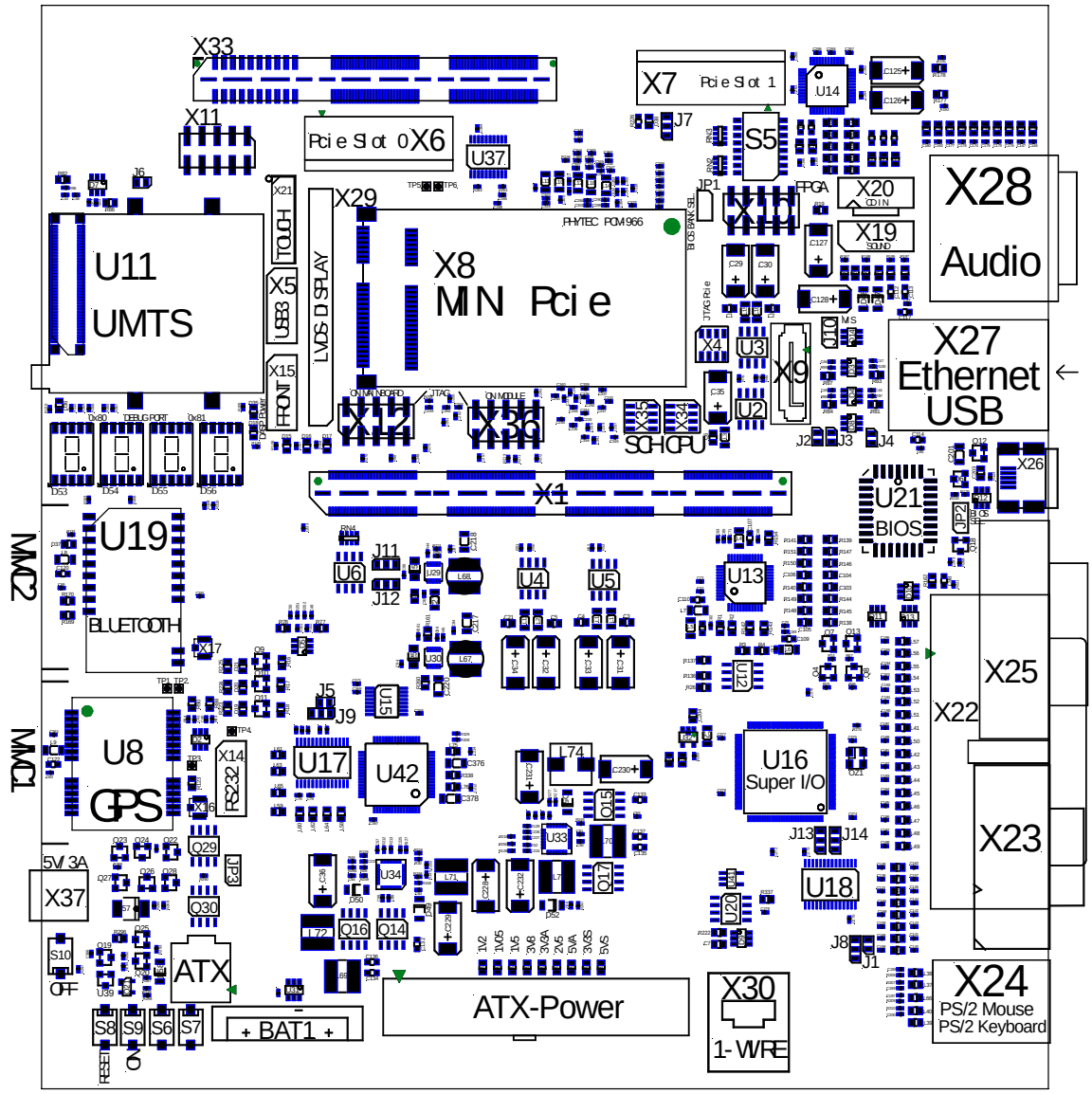


Figure 12: Top view of the phyCORE-Z500P(T) Carrier Board

11.3.1 Module Connector (X1)

The phyCORE-Z500P(T) must be placed correctly onto the Carrier Board at X1. Be careful when pushing down the module. It is possible to bolt the module at the baseboard with 8 mm bolts.

11.3.2 Power Supply (X37) / ATX-Power

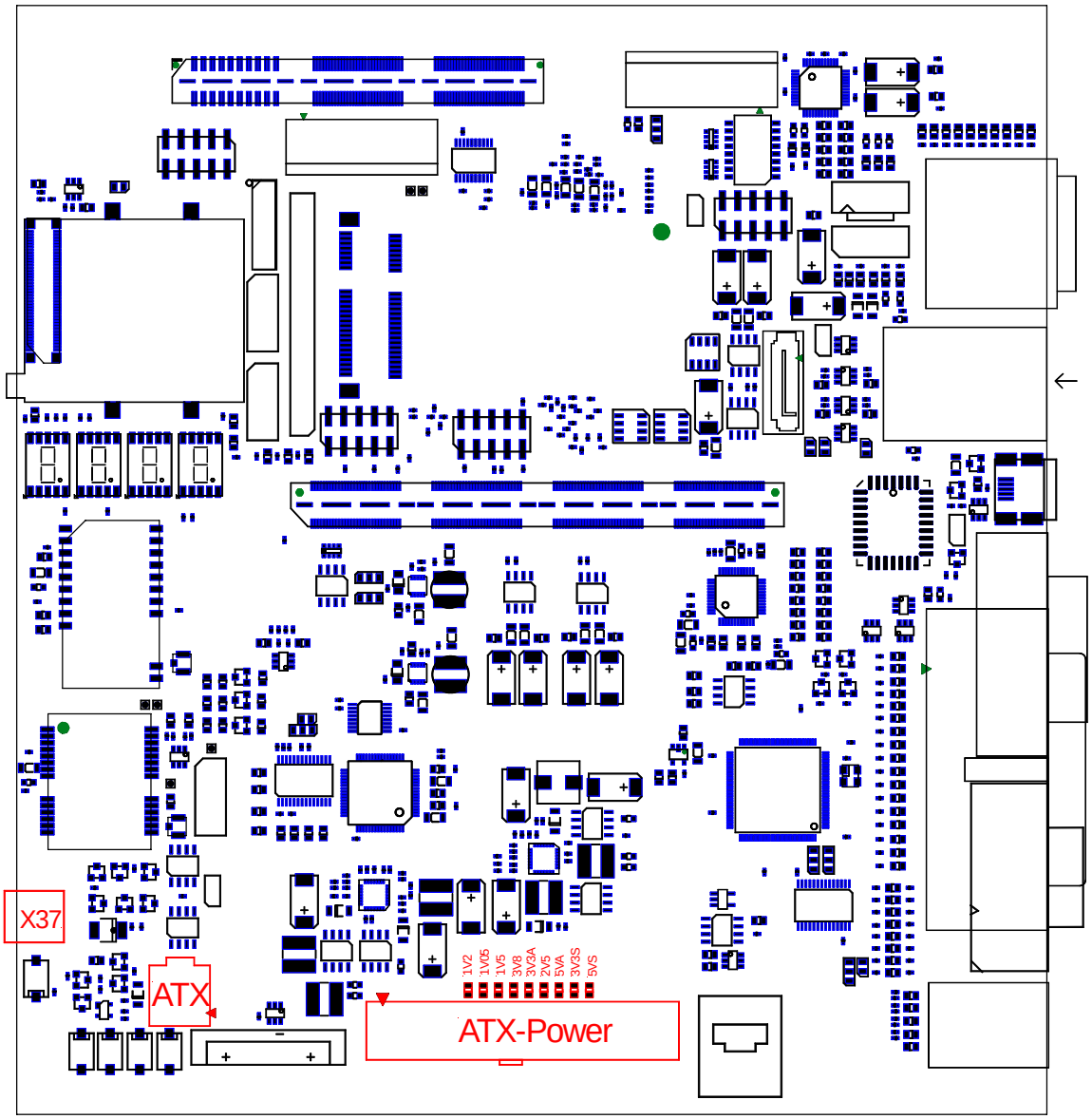


Figure 13: Power Supply (X37)

Caution!
Do not use a laboratory adapter to supply power to the baseboard!
Power spikes during power-on could destroy the phyCORE module mounted on the baseboard!
Do not change modules or jumper settings while the baseboard is supplied with power!

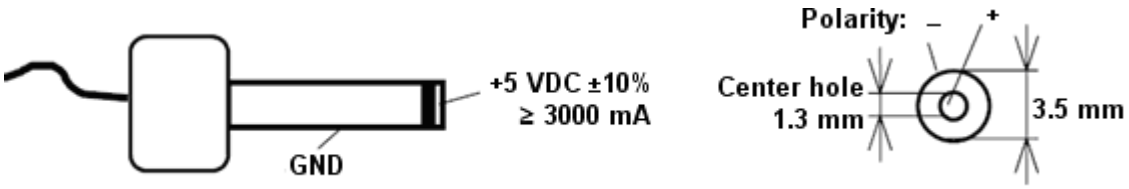


Figure 14: Power adapter

The Carrier Board can be powered either with an external Power adapter 5 VDC/3000 mA or an standard ATX power supply. If an ATX power supply is connected the Power adapter is electronically disconnected.

A battery (BAT1) is used as backup supply for CMOS and other nonvolatile components on the module.

Fore ease to see which voltage is powered on/off, there are LED's above the ATX-Power connector.

11.4 USB

The phyCORE-Z500P(T) provide eight USB ports. Two of them (Port 6 and 7) are only internally connected to the EHCI controller and therefore limited to High-Speed. USB Port 2 is capable to be used as USB-Client.
At the phyCORE-Z500P(T) Carrier Board the USB Ports are connected to on board devices like UMTS, GPS, QUAD-UART (FTDI)

USB-Port	Usage
0	Bottom USB connector at (X27)
1	Top USB connector (X27)
2	USB-OTG (X26)
3	Pinheader X5 / miniPCIe-Slot (X8) / LVDS-Display connector (X29)
4	UMTS (U11)
5	GPS (U8)
6	Pinheader X5 (only High-Speed)
7	Quad UART FTDI (U42)

Table 9: USB Port usage

11.4.1 USB-Host connector (X27)

At connector X27 USB-Port 0 and 1 are available for use with standard USB devices like USB-Storage, USB-Mouse, USB-Keyboard and other USB compliant devices. Both Ports have a maximum output current of 500mA. This is supervised by an TPS2042A device (U3). If an over current situation occurs, the power is switched of and signaled to the SCH

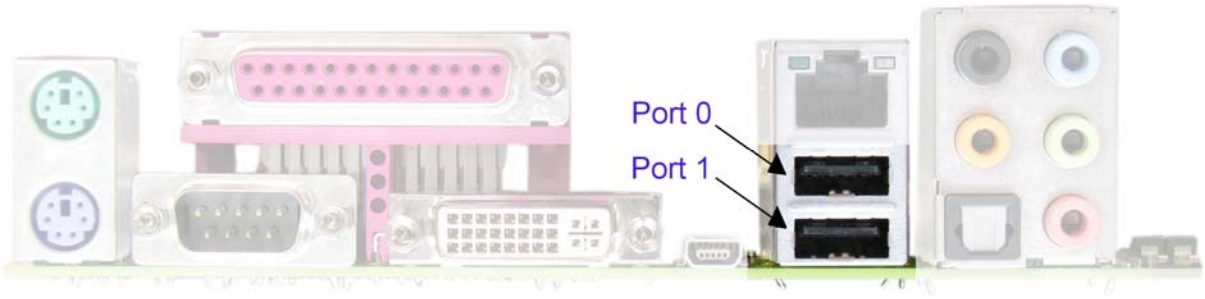


Figure 15: USB-Host connector Port-0/1

Pin	Signal
1	VUSB
2	USB D+
3	USB D-
4	GND

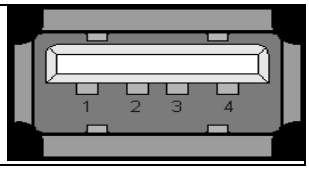


Table 10: Pinning of X27

11.4.2 USB-Host/Client (X26)

The Intel SCH supports the USB-Client or USB-Host feature on Port 2. The connector type of X26 is USB Mini AB.

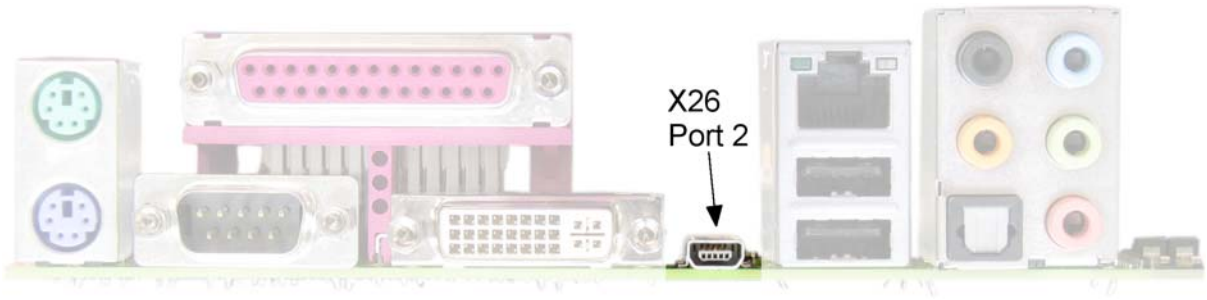


Figure 16: USB-OTG (X26)

Pin	Signal
1	VBUS
2	USB D-
3	USB D+
4	ID
5	GND

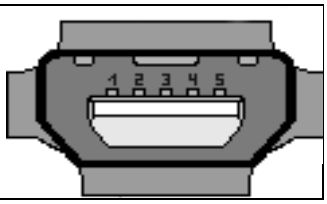


Table 11: Pinning of X26

11.4.3 USB-Pin Header X5

The USB-Ports 3 and 6 are available at the pin header X5. The pinning is compatible with the Intel "Front Panel I/O Connectivity Design Guide" (v1.2). Both ports are able to supply up to 500mA to the connected USB-Device.

Remark:
USB-Port 6 is only capable for High-Speed connections

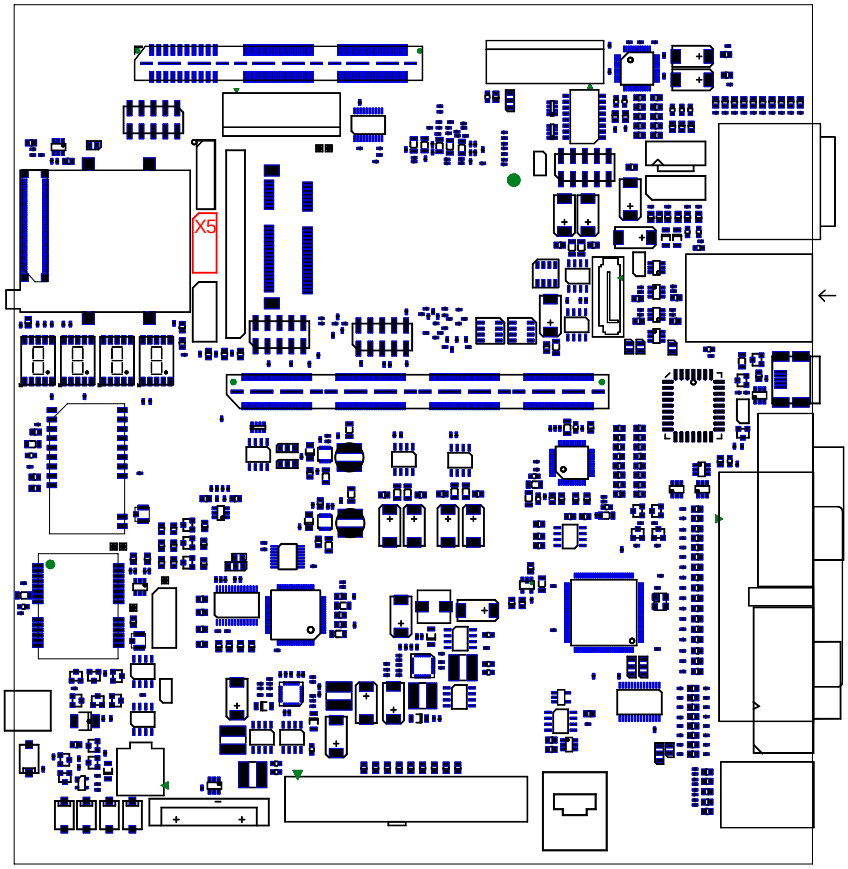


Figure 17: USB-Pin Header X5

Pin	Signal
1	VCC_USB3
2	VCC_USB6
3	USB_DN_3_CON
4	USB_DN_6_CON
5	USB_DP_3_CON
6	USB_DP_6_CON
7	GND
8	GND
9	n.c. (key)
10	n.c.

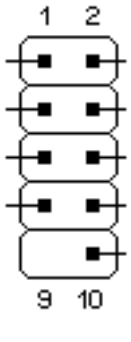


Table 12: Pinning of USB-Pin Header X5

11.5 UMTS (U11)

At position U11, a UC864 UMTS module (and compatible) from Telit can be mounted. This gives the ability for a wide range of communication.
The module is connected to the phyCORE-Z500P(T) via USB port 4 at full speed. There is also a serial connection via the Super-I/O (U16) at serial2.
For voice function, the analog sound signals are connected to the Analog-Devices HDA sound chip (U14) and the digital (PCM) signals are connected to the Bluetooth module (U19).

Audio-Signal	Function	direction	Connected to
EAR_HF+	Hands-free ear output, phase +	Analog out	Phone_in (U14)
MIC_HF+	Hands-free microphone input; phase +	Input	Mono_Out (U14)
PCM_CLOCK_BT	PCM clock out	Input/Output	SCLK Bluetooth (U19)
PCM_RX_BT	PCM Data input	Input	SRD Bluetooth (U19)
PCM_TX_BT	PCM Data output	Output	STD Bluetooth (U19)
PCM_SYNC_BT	PCM Sync	Input/Output	SFS Bluetooth (U19)

A SIM-Card must be plugged in at X18 on the bottom side of the phyCORE-Z500P(T) baseboard, to connect to your service provider. There are several control signals from/to the UMTS module which are described in the following table.

Signal	Function	direction	Connected to
UMTS_ON_OFF	Power on/off	Input	Output of EPLD (U35)
UMTS_RESET	Reset	Input	Output of EPLD (U35)
UMTS_PWRMON	Power Monitor	Output	Input of EPLD (U35)

Led D36 signals the status of the UMTS module/connection. *For further information see the Users-Manual/Datasheet of the mounted module at www.telit.com.*

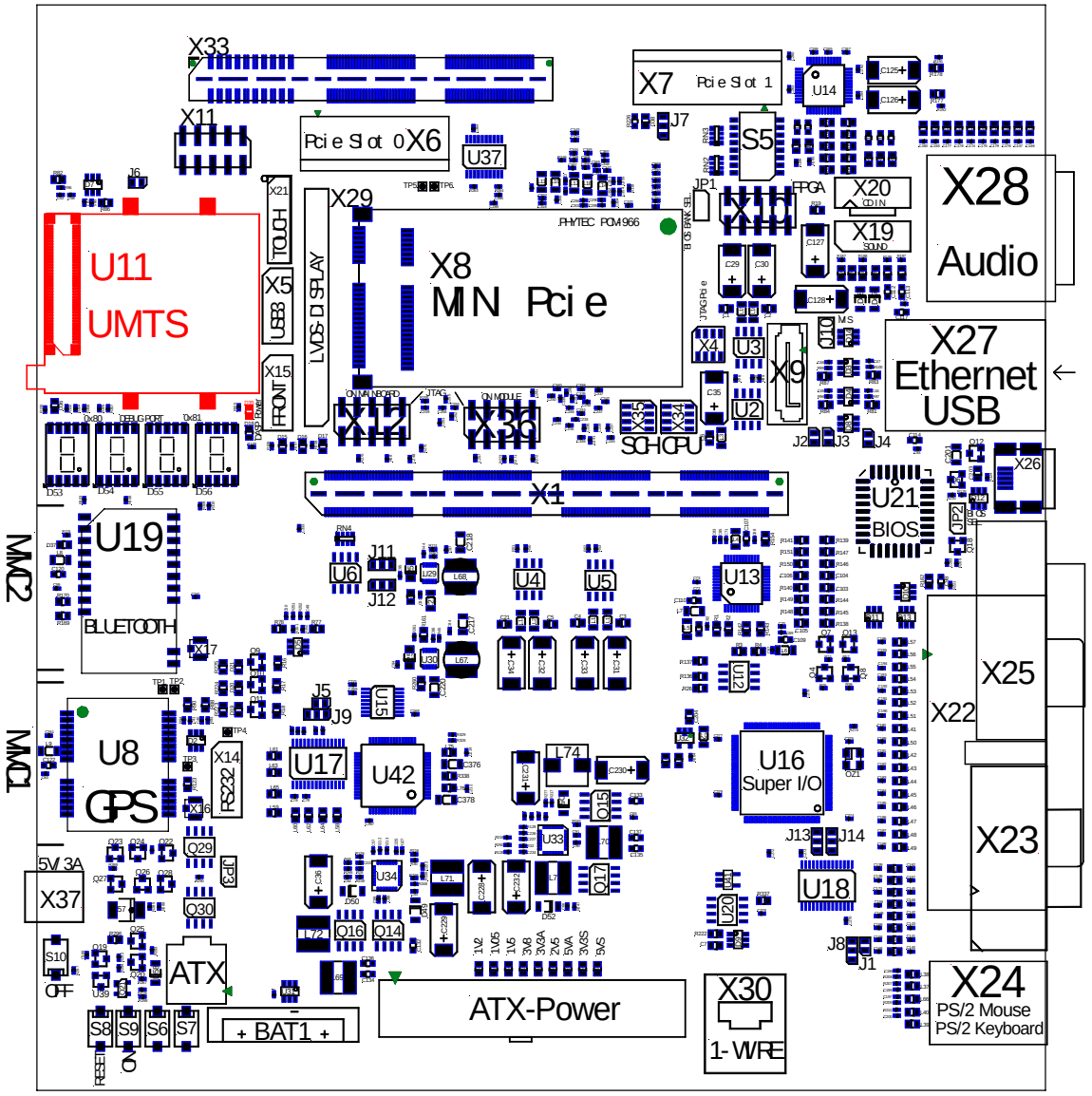


Figure 18: UMTS (U11)

11.6 GPS (U8)

A ublox LEA-5H GPS receiver can be populated at position U8. This GPS receiver can be accessed by I²C or USB (connected to USB-Port 5) at full speed. The default I²C/DDC address is 0x42.
It is possible to connect an external antenna at X16.
For further information on Hardware or Software related issues, *refer the datasheets/user-manuals at www.u-blox.com.*

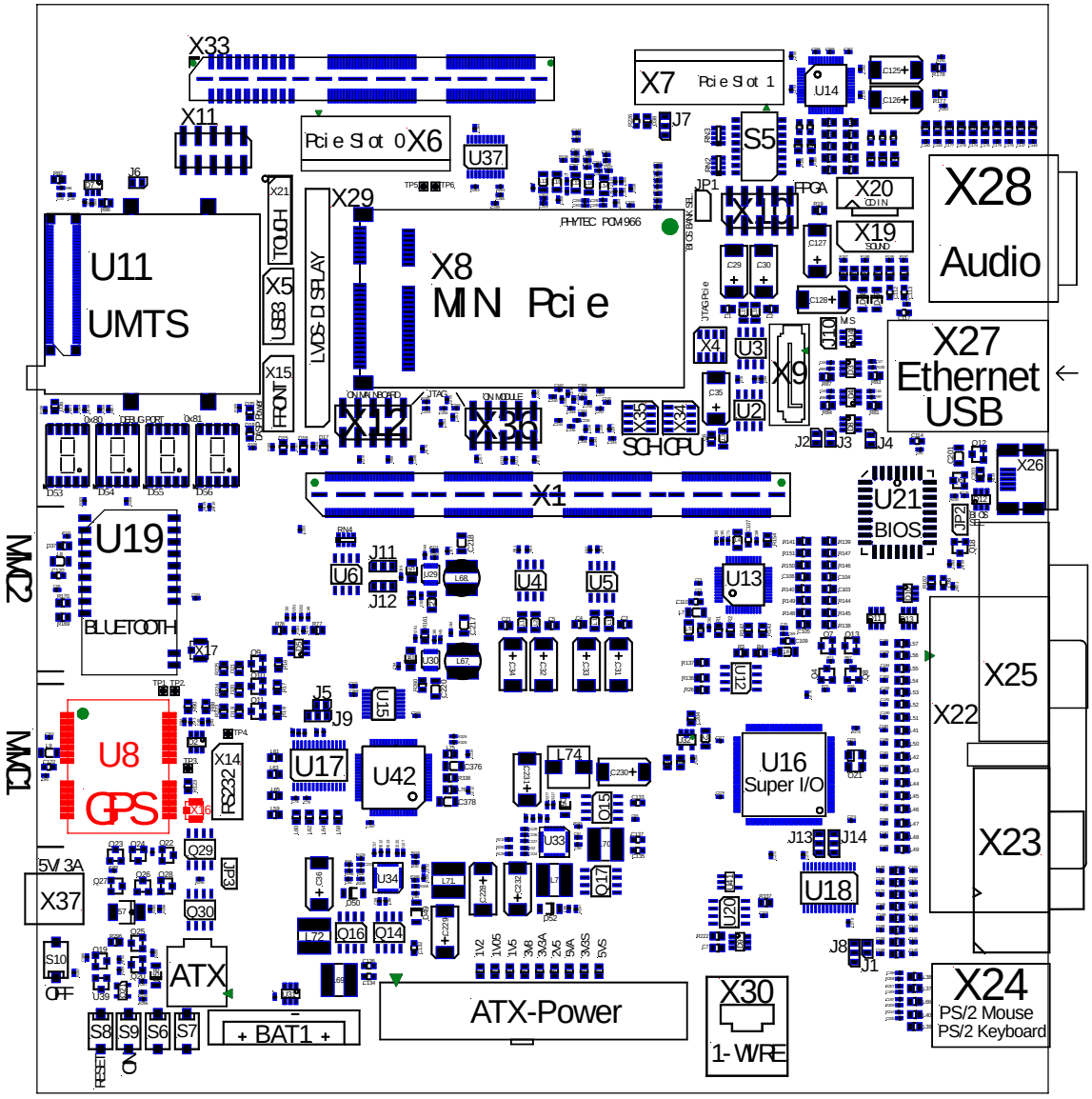


Figure 19: GPS (U8)

11.7 RS-232 Pin header (X14)

Pin header X14 provides a connection to a serial interface (RS232 level) of the quad FTDI U14 which is connected at high-speed to USB port 7 of the phyCORE-Z500P(T). The pin out is designed to match with a MALE DSUB 9 connector using a flat ribbon cable.

Pin	Signal	Direction
1	DCD6_RS232_CON	Input
2	DSR6_RS232_CON	Input
3	RXD6_RS232_CON	Input
4	RTS6_RS232_CON	Output
5	TXD6_RS232_CON	Output
6	CTS6_RS232_CON	Input
7	DTR6_RS232_CON	Output
8	RI6_RS232_CON	Input
9	GND	Power
10	n.c. (key)	

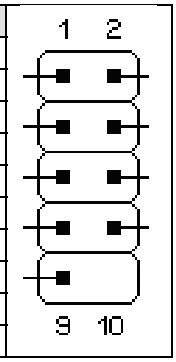


Table 13: Pinning of RS232-Pin Header X14

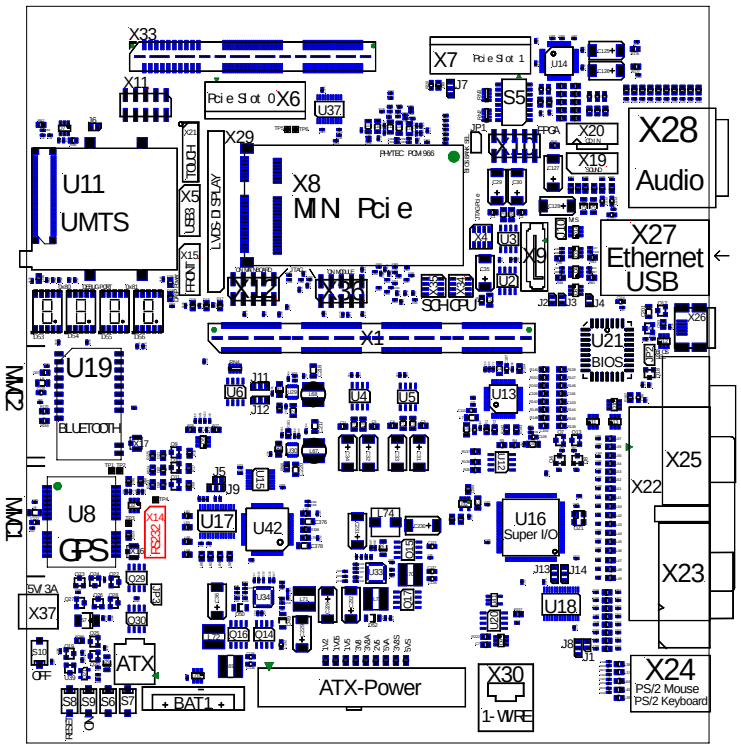


Figure 20: RS232 Pin Header X14

11.8 One-Wire Interface (X30)

The RJ11 connector X30 provides a connection to the phyCORE-Z500P(T) baseboard One-Wire serial interface. This interface is realized by an serial to One-Wire converter DS2480B which is connected to serial port 3 of the FTDI U14 which is connected at high-speed to USB port 7 of the phyCORE-Z500P(T).
The One-Wire bus system was designed by Dallas Semiconductor and provides low-speed data, signaling, and power over a single wire (a ground wire is also needed). One-Wire is similar in concept to I²C, but with lower data rates and a much lower cost. It is typically used to communicate with small inexpensive devices such as digital thermometers and weather instruments.

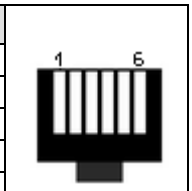
PIN NUMBER	SIGNAL NAME	FUNCTION	
1	VCC5VA	Power supply for One-Wire	
2	GND	Ground	
3	1_WIRE_CON	Data	
4	GND	Ground	
5	Not connected	n/a	
6	Not connected	n/a	

Table 14: One-Wire connector

Note:
Many One-Wire devices operate within a voltage range of 2.8 V to 5.5 V. But there are also some devices which only operate from 3 V to 3.7 V. Please refer to the datasheet of the One-Wire device which should be used to avoid destruction.

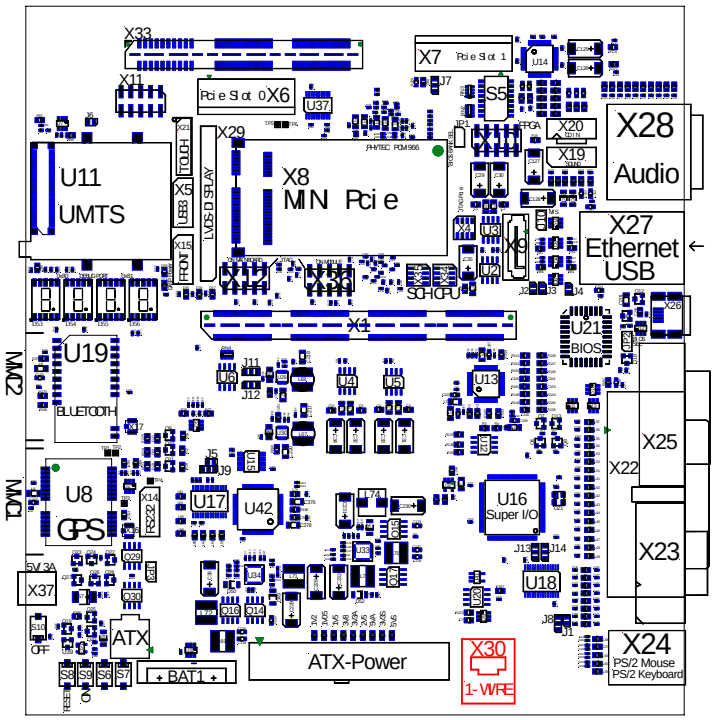


Figure 21: One-Wire connector X30

11.9 Bluetooth Interface (U19)

The phyCORE-Z500P(T) baseboard is also equipped with a Bluetooth module called 'BlueNiceCom 4' from AMBER wireless (www.amber-wireless.de).
This module is connected to serial port 4 of the FTDI U14 which is connected at high-speed to USB port 7 of the phyCORE-Z500P(T). The PCM audio signals are connected to the UMTS module (U11), so it is possible to use the Bluetooth audio part. LED D37 lights up if traffic is detected.
It is possible to connect an external antenna to X17. Therefore the module must be modified. *For further information see the datasheet/users-manual at www.amber-wireless.com.*

The Baud rate after power-up can be selected with R169/R170 according the following table:

Baudrate	R169 (OP4)	R170 (OP5)
Read from int. EERPOM	populated	populated
9600 bps	---	populated
115200 bps	populated	---
921600 bps	populated	populated

Table 15: Bluetooth baudrate

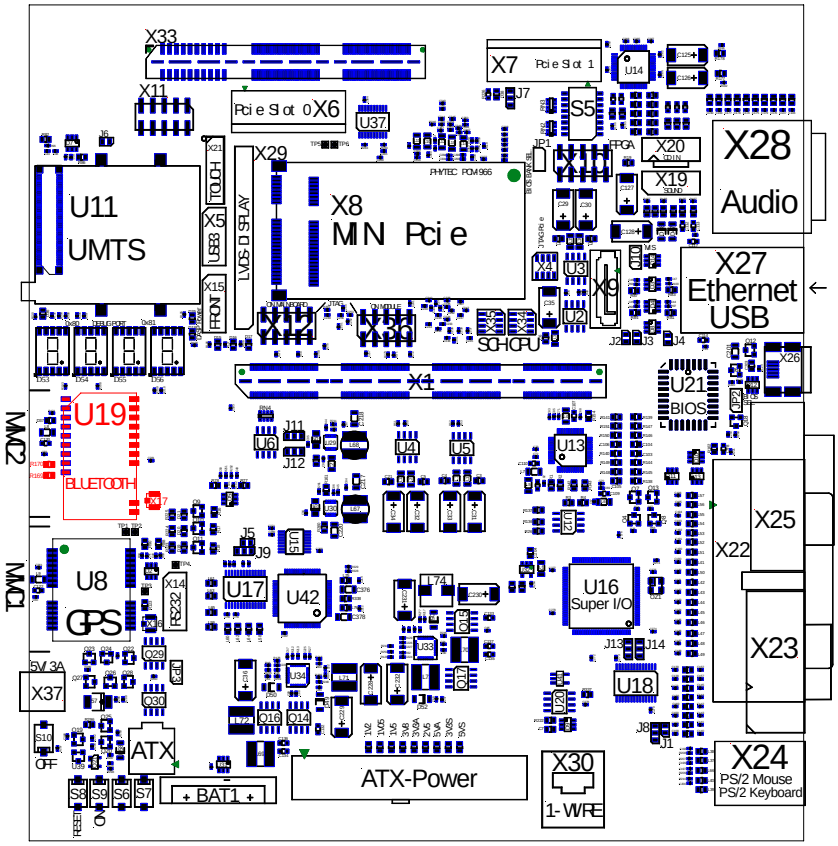


Figure 22: Bluetooth module (U19)

11.10 Touch connector X21

An ADS7845 touch controller (U15) is connected to serial port 1 of the FTDI U14 which is connected at high-speed to USB port 7 of the phyCORE-Z500P(T). This port is used in SPI mode. The touch signals are available at X21 and X29.

Signal	X21	X29
UL	1	35
UR	2	33
LL	3	36
LR	4	34
WIPER	5	38

Table 16: Touch signals at X21/X29

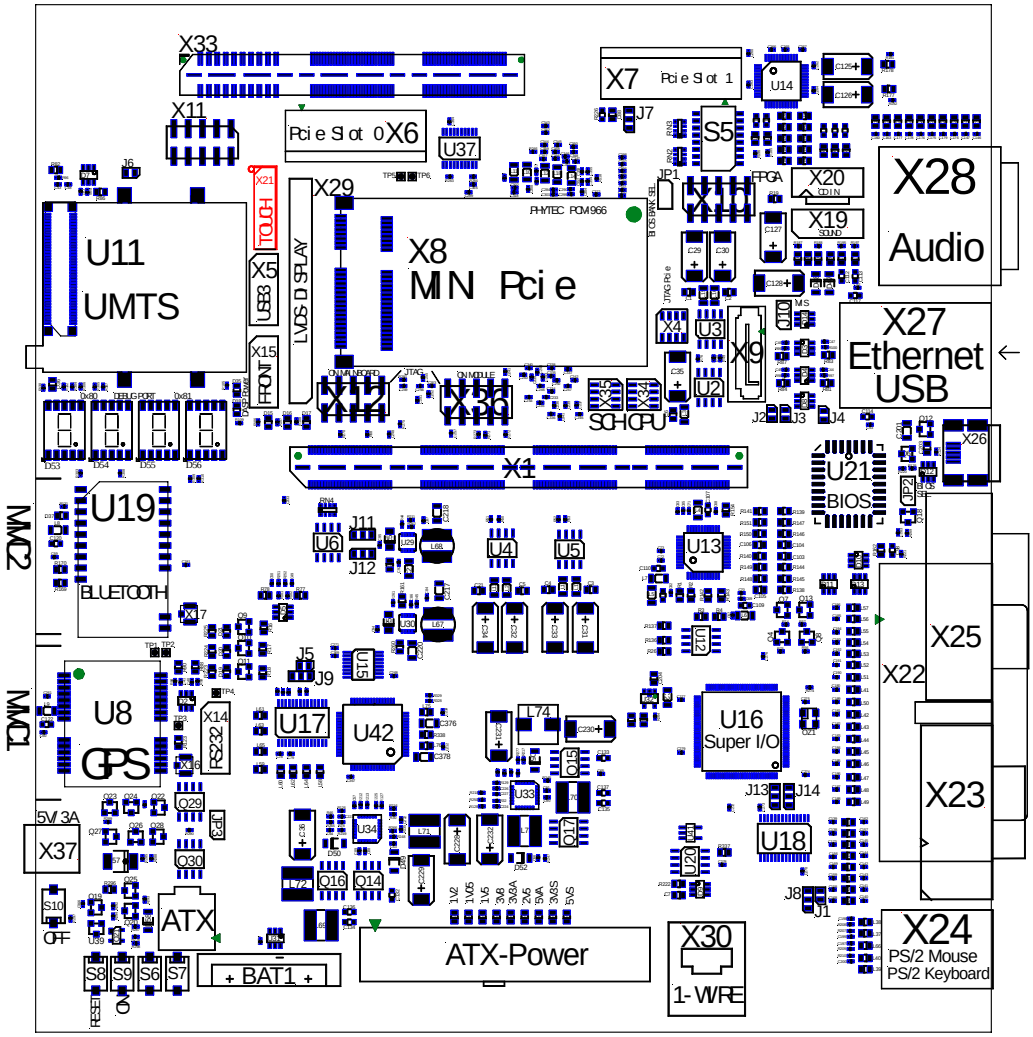


Figure 23: Touch connector X21

11.11 RS-232 Interface (X23)

Connector X23 provides a connection to the first Super-IO (SMSC3112) serial interface (RS232 level). The RS232 interface (X23) provides a full set of handshake signals at RS-232 compatible levels.

Table 17: RS-232 Interface X23

below shows the signal mapping of the RS-232 level signals to connector X23.
This serial interface can be accessed through Uart1 at IO-address 0x3f8 IRQ4.

Pin	Signal	Direction
1	DCD1_RS232_CON	Input
2	DSR1_RS232_CON	Input
3	RXD1_RS232_CON	Input
4	RTS1_RS232_CON	Output
5	TXD1_RS232_CON	Output
6	CTS1_RS232_CON	Input
7	DTR1_RS232_CON	Output
8	RI1_RS232_CON	Input
9	GND	Power
10	n.c. (key)	

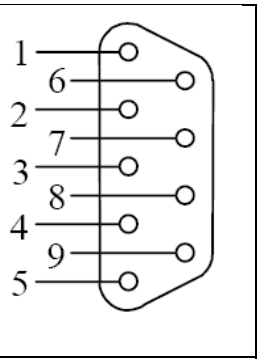


Table 17: RS-232 Interface X23

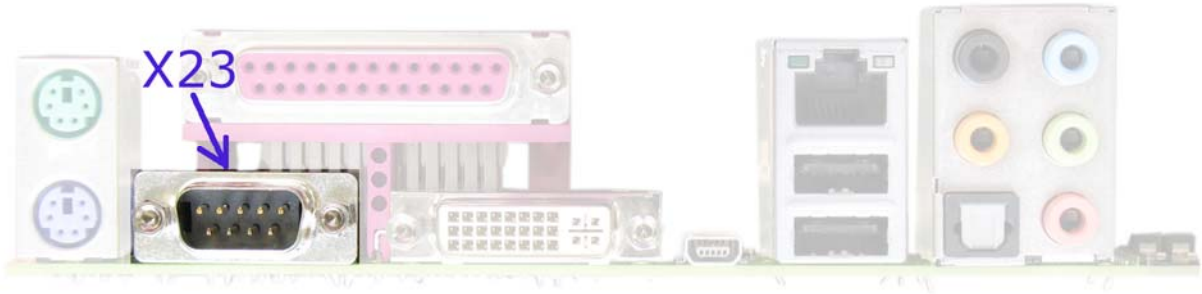


Figure 24: RS232 Interface X23

11.12 LPT Printer Interface (X22)

The female connector X22 provides a connection to the Super-IO (SMSC3112) parallel port (LPT) interface (TTL Level). *Table 18 b*elow shows the signal mapping of the LPT signals to connector X22. This LPT interface can be accessed at IO-address 0x378 IRQ5.

Pin	Signal	Direction
1	#STROBE_CON	Output
2	PD0_CON	I/O
3	PD1_CON	I/O
4	PD2_CON	I/O
5	PD3_CON	I/O
6	PD4_CON	I/O
7	PD5_CON	I/O
8	PD6_CON	I/O
9	PD7_CON	I/O
10	#ACK_CON	Input
11	BUSY_CON	Input
12	PE_CON	Input
13	SLCT_CON	Input
14	#ALF_CON	Output
15	#ERROR_CON	Input
16	#INIT_CON	Output
17	#SLCTIN_CON	Output
18	GND	Power
19	GND	Power
20	GND	Power
21	GND	Power
22	GND	Power
23	GND	Power
24	GND	Power
25	GND	Power

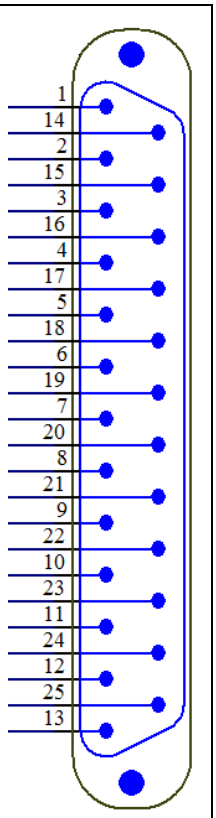


Table 18: LPT interface (X22)

Figure 25: LPT Printer Interface X22

11.13 PS/2 Mouse/Keyboard interface (X24)

Connector X24 provides a connection to the Super-IO (SMSC3112) Mouse and Keyboard interface (TTL Level). *Table 19* below shows the signal mapping of the signals to connector X24.
This Keyboard uses IRQ1 and Mouse IRQ12.

Pin	Signal	Direction
1	PS/2_KEYB_DAT_CON	I/O
2	N.C.	---
3	GND	Power
4	VCC5VA	Power
5	PS/2_KEYB_CLK_CON	I/O
6	N.C.	---
7	PS/2_MOUSE_DAT_CON	I/O
8	N.C:	---
9	GND	Power
10	VCC5VA	Power
11	PS/2_MOUSE_CLK_CON	I/O
12	N.C:	---

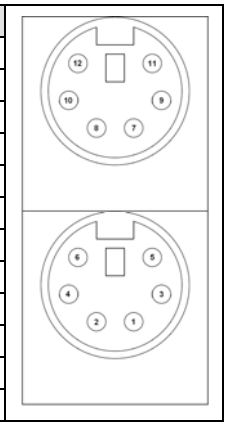


Table 19: PS/2 Mouse and Keyboard interface (X24)

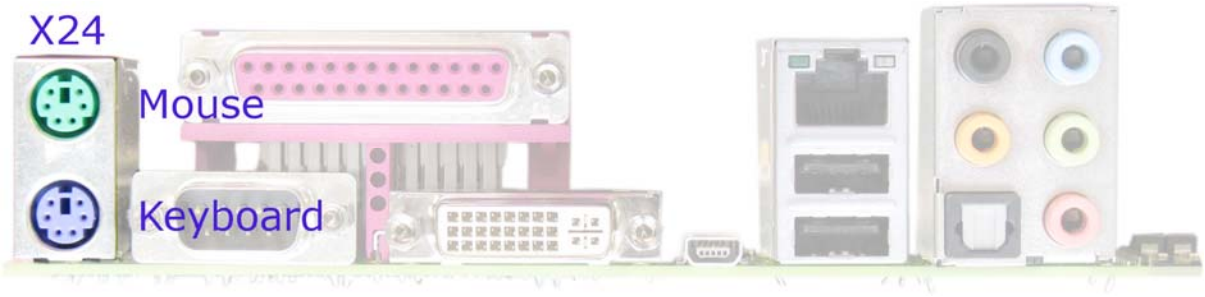


Figure 26: PS/2 Mouse and Keyboard interface (X24)

11.14 DVI-I Video interface (X25)

Connector X25 provides a connection to the DVI video output of the SDVO chip CH7307C from Chrontel.

Pin	Signal	Direction
1	DVI_D2_N	Diff out
2	DVI_D2_P	Diff out
3	GND	Power
4	N.C.	---
5	N.C.	---
6	DDC_CLK	I/O
7	DDC_DATA	I/O
8	N.C.	---
9	DVI_D1_N	Diff out
10	DVI_D1_P	Diff out
11	GND	Power
12	N.C.	---
13	N.C.	---
14	VCC5VA	Power
15	GND	Power
16	HPDET	Input
17	DVI_D0_N	Diff out
18	DVI_D0_P	Diff out
19	GND	Power
20	N.C.	---
21	N.C.	---
22	GND	Power
23	DVI_CLK_P	Diff out
24	DVI_CLK_N	Diff out
C1	N.C.	---
C2	N.C.	---
C3	N.C.	---
C4	N.C.	---
C5	N.C.	---

Table 20 below shows the signal mapping of the signals to connector X25.

Pin	Signal	Direction
1	DVI_D2_N	Diff out
2	DVI_D2_P	Diff out
3	GND	Power
4	N.C.	---
5	N.C.	---
6	DDC_CLK	I/O
7	DDC_DATA	I/O
8	N.C.	---
9	DVI_D1_N	Diff out
10	DVI_D1_P	Diff out
11	GND	Power
12	N.C.	---
13	N.C.	---
14	VCC5VA	Power
15	GND	Power
16	HPDET	Input
17	DVI_D0_N	Diff out
18	DVI_D0_P	Diff out
19	GND	Power
20	N.C.	---
21	N.C.	---
22	GND	Power
23	DVI_CLK_P	Diff out
24	DVI_CLK_N	Diff out
C1	N.C.	---
C2	N.C.	---
C3	N.C.	---
C4	N.C.	---
C5	N.C.	---

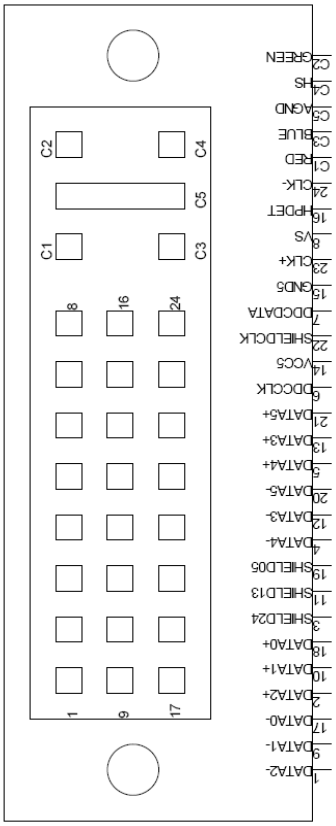


Table 20: DVI-I connector X25

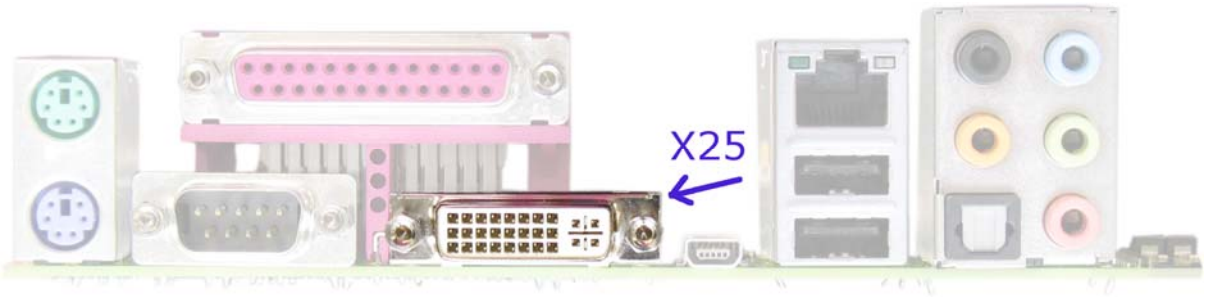


Figure 27: DVI-I connector X25

11.15 Ethernet Interface (X27)

Connector X27 provides a connection to the 1-GB/s Ethernet interface of the Intel 82574 Ethernet controller on the phyCORE-Z500P(T). *Table 21* below shows the signal mapping of the signals to connector X27.
LED1 (green) acts as the link status LED and LED2 as traffic.

Pin	Signal
J1	MDI_CS0P
J2	MDI_CS0N
J3	MDI_CS1P
J4	MDI_CS1N
J5	MDI_CS2P
J6	MDI_CS2N
J7	MDI_CS3P
J8	MDI_CS3N

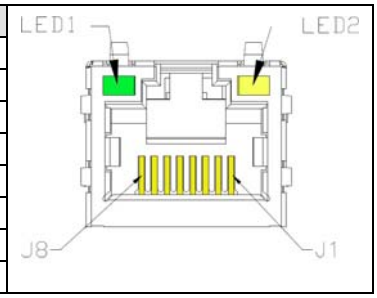


Table 21: Ethernet interface X27

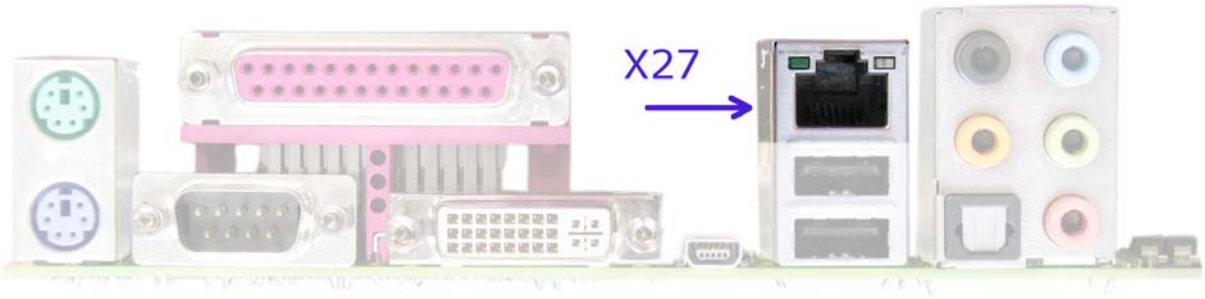


Figure 28: Ethernet Interface X27

11.16 Audio connector (X28)

Connector X28 provides a connection to the different audio signals from the AD1986A from Analog Devices. *Table 22* below shows the signal mapping of the signals to connector X28.

Color	Signal	
Black	Center Out	
Blue	Line In	
Orange	Surround Out	
Green	Line Out	
Pink	Micro	
Square black/grey	Optical Interface	

Table 22: Audio connector X28

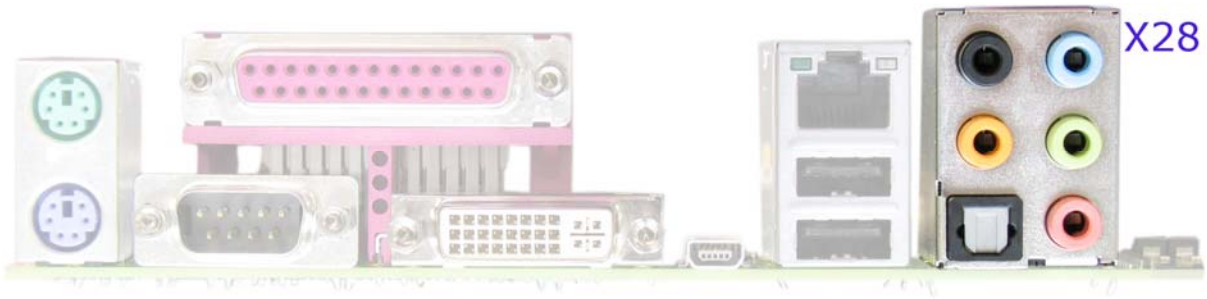


Figure 29: Audio connector X28

11.17 Front-Panel Pin header (X15)

Pin header X15 provides a connection to different signals, which can be used at a typical PC front panel like hard drive activity LED, Power-Led, Reset and Wakeup.

Pin	Signal	Description
1-3	Hard Drive activity	Connect a LED between pin 1(anode) and pin 3(cathode).
2-4	Power-LED	Connect a LED between pin 2(anode) and pin 4(cathode).
5-7	Reset-Button	Connect a reset button between pin 5 (#PM_SYSRST) and Pin 7 (GND)
6-8	Power-Button	Connect a power button between pin 6 (#PWR_BTN) and Pin (GND)
9	N.C.	Power
10	N.C. (Key)	

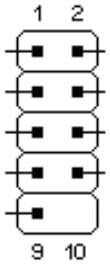


Table 23: Front Panel Pin Header X15

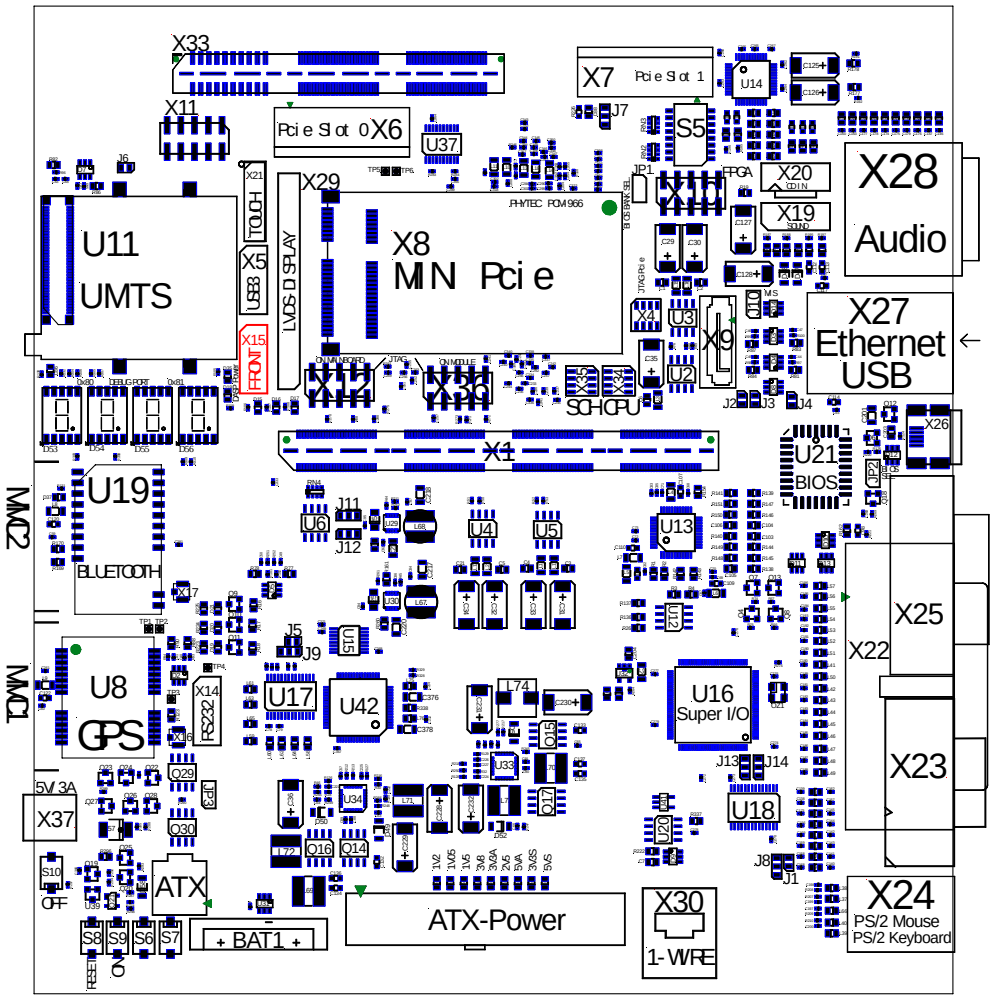


Figure 30: Front Panel Pin Header X15

11.18 Audio-Signal Pin header (X19)

Pin header X19 provides a connection to different audio signals. *Table 24* below shows the signal mapping of the signals to connector X19.

Pin	Signal	Description
1	MIC_1	Microphone input 1
2	GND	Ground
3	MIC_2	Microphone input 2
4	Front_Presense	Frontpanel presense detection input. Pull down to activate.
5	HEADPHONE_R	Right Headphone input
6	MIC1/2_JD	Microphone 1/2 detection input
7	GND	Ground
8	N.C. (Key)	
9	HEADPHONE_L	Left Headphone input
10	HP_OUT_JD	Headphone detection input

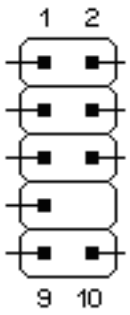


Table 24: Audio Signal Pin header X19

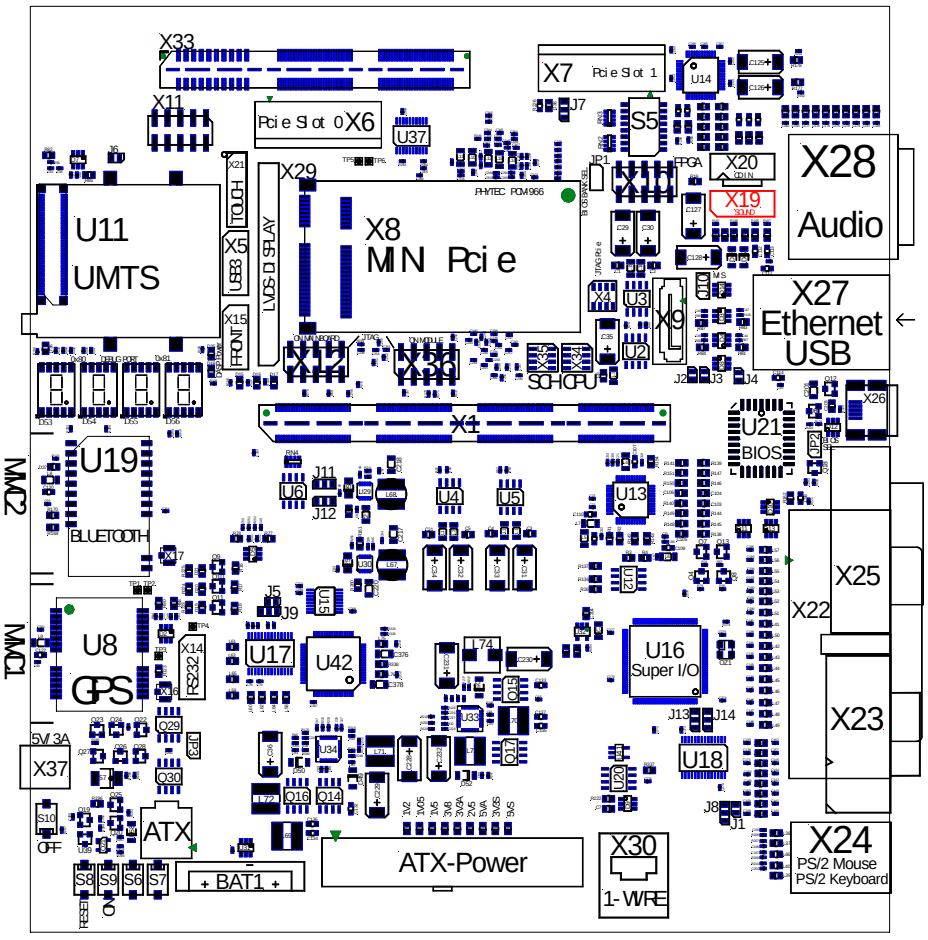


Figure 31: Audio Signal Pin Header X19

11.19 CD-Audio-connector (X20)

At Pin header X20 you can connect the audio output of a CDROM drive. *Table 25* below shows the signal mapping of the signals to connector X20.

Pin	Signal	Description
1	MIC_1	Microphone input 1
2	GND	Ground
3	MIC_2	Microphone input 2
4	Front_Presense	Front panel presence detection input. Pull down to activate.
5	HEADPHONE_R	Right Headphone input
6	MIC1/2_JD	Microphone 1/2 detection input
7	GND	Ground
8	N.C. (Key)	
9	HEADPHONE_L	Left Headphone input
10	HP_OUT_JD	Headphone detection input

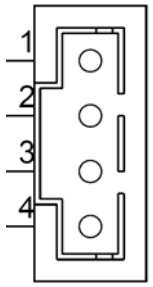


Table 25: CD-Audio connector X20

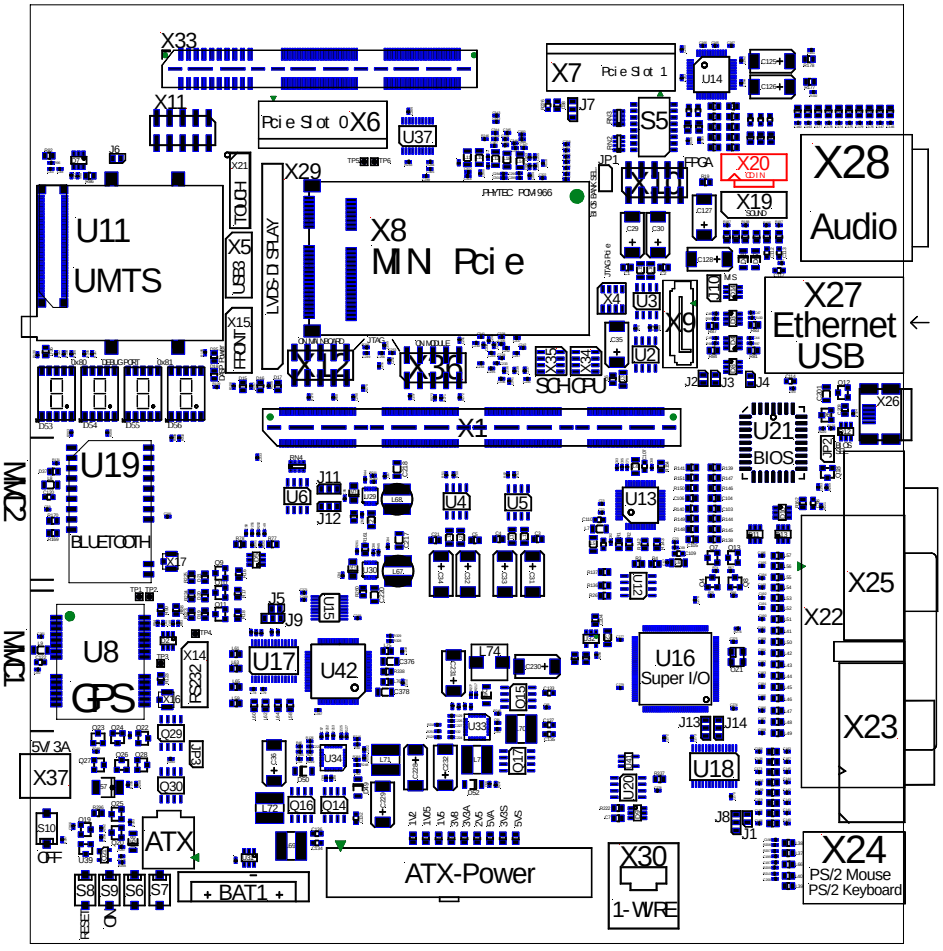


Figure 32: CD-Audio connector X20

11.20 SATA-connector (X9)

A SATA connector provides the possibility to connect an external SATA hard drive to the phyCORE-Z500P(T). *Table 26* below shows the signal mapping of the SATA connector X9.

Pin	Signal	Description
1	GDN	Microphone input 1
2	SATA_TX	Ground
3	#SATA_TX	Microphone input 2
4	GND	Front panel presence detection input. Pull down to activate.
5	#SATA_RX	Right Headphone input
6	SATA_RX	Microphone 1/2 detection input
7	GND	Ground

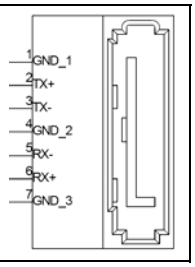


Table 26: SATA connector X9

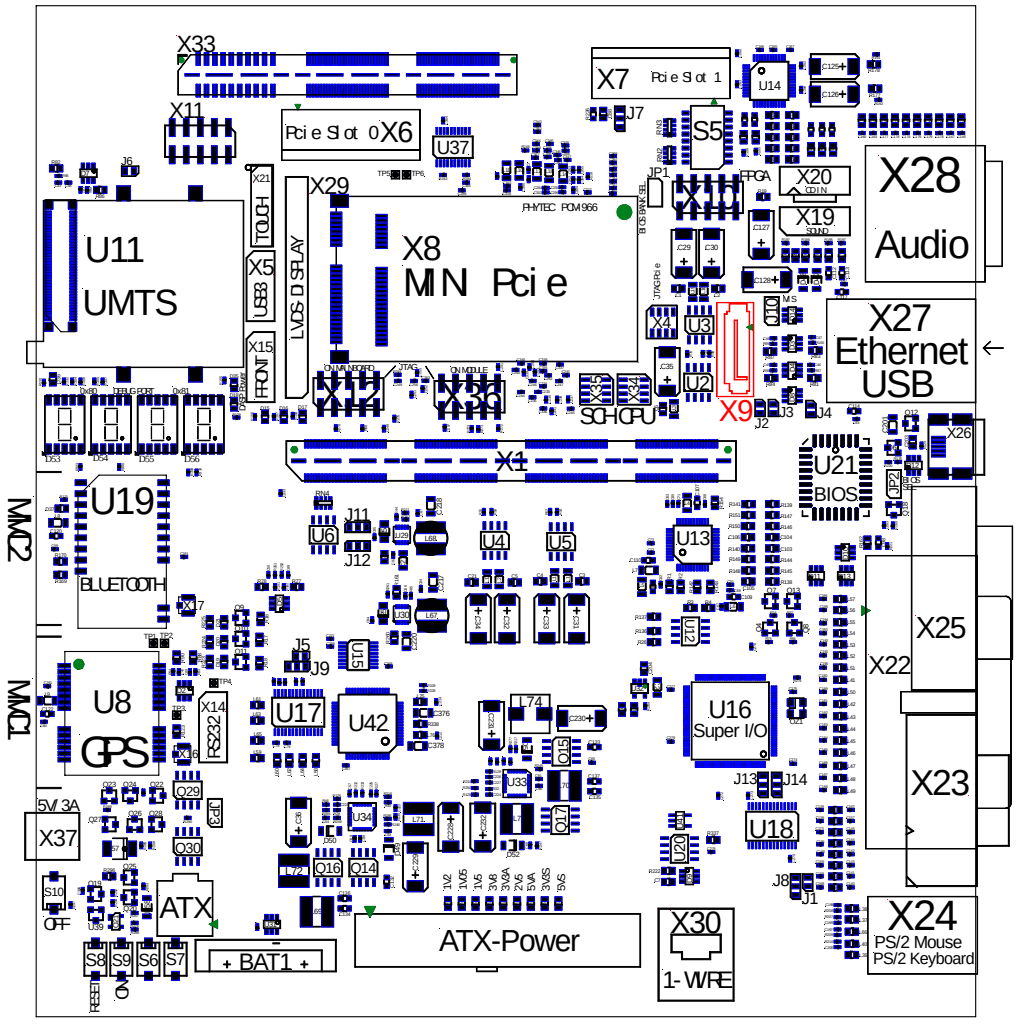


Figure 33: SATA connector X9

11.21 Universal LVDS Display pinheader (X29)

Pin header connector X29 provides a connection to the phyCORE-Z500P(T) LVDS display interface. *Table 27* provides a detailed list of the signals found at X29.

Pin	Signal	Description
1	GDN	Microphone input 1
2	SATA_TX	Ground
3	#SATA_TX	Microphone input 2
4	GND	Front panel presence detection input. Pull down to activate.
5	#SATA_RX	Right Headphone input
6	SATA_RX	Microphone 1/2 detection input
7	GND	Ground

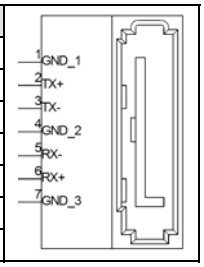


Table 27: Universal LVDS Display pin header X29

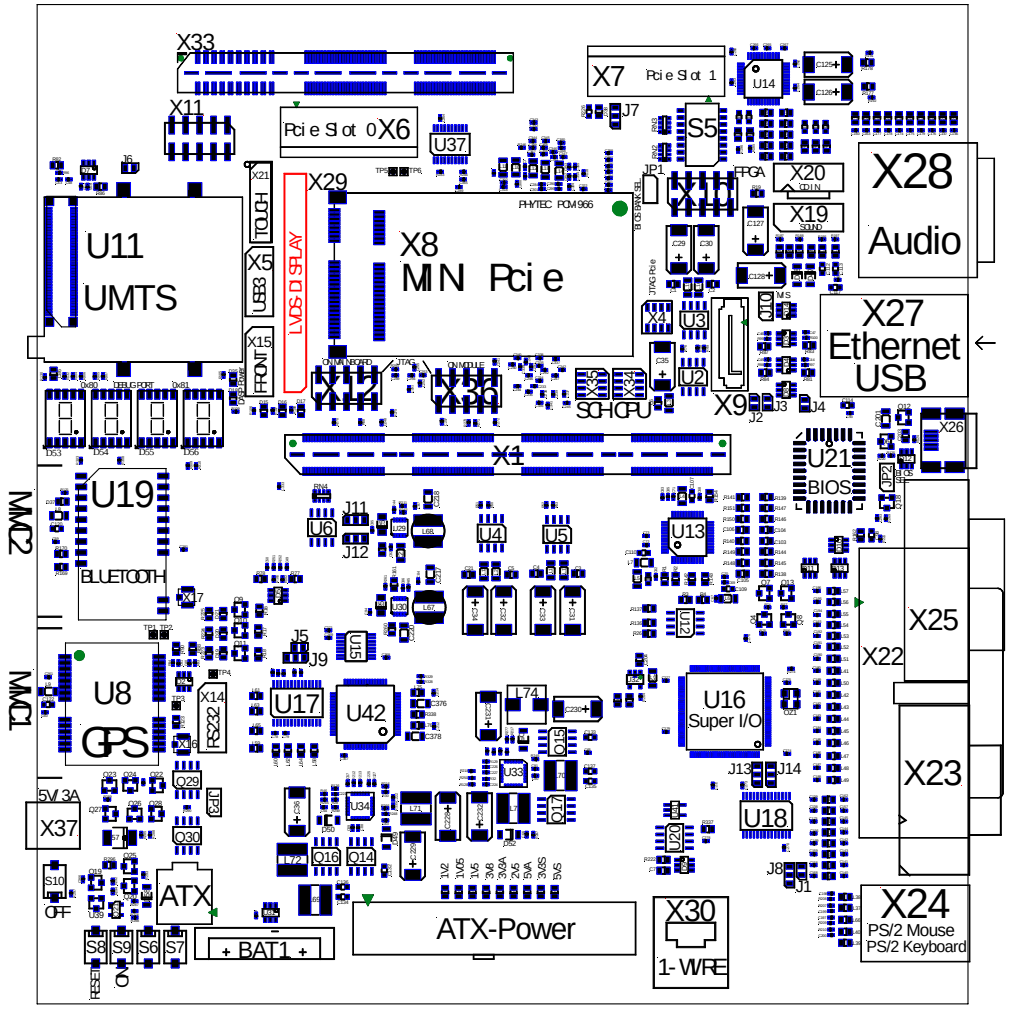


Figure 34: Universal LVDS Display pin header X29

11.22 Secure Digital / Multi-Media Card (X31/X32)

Two Security Digital interfaces are available on the bottom side of the phyCORE-Z500P(T) baseboard at X31 and X32.*Table 28* provides a detailed list of the signals found at X31 and X32.
Both connectors are powered via power switch U6, which is used to power On/Off the sockets by the #MMC1/2_PWR signal or by inserting a SD/MMC card. The maximum current per port is limited to 500 mA.

Pin	Signal	Description	On board
1	MMC1_DATA3	Dataline 3	
2	MMC1_CMD	Command	PU10k
3	GND	Ground	
4	VCC3V3S	Power	
5	MMC1_CLK	Clock	PU10k
6	GND	Power	
7	MMC1_DATA0	Dataline 0	
8	MMC1_DATA1	Dataline 1	
9	MMC1_DATA2	Dataline 2	
10	#MMC1_CD	Card detect	
11	GND	Ground	
12	MMC1_WP	Write-Protect	PU10k

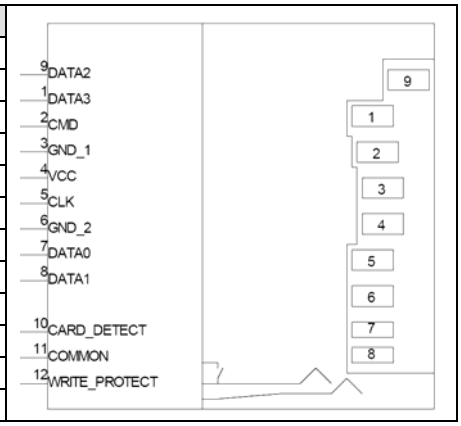


Table 28: Secure Digital / Multi-Media-Card X31

Pin	Signal	Description	On board
1	MMC2_DATA3	Dataline 3	
2	MMC2_CMD	Command	PU10k
3	GND	Ground	
4	VCC3V3S	Power	
5	MMC2_CLK	Clock	PU10k
6	GND	Power	
7	MMC2_DATA0	Dataline 0	
8	MMC2_DATA1	Dataline 1	
9	MMC2_DATA2	Dataline 2	
10	#MMC2_CD	Card detect	
11	GND	Ground	
12	MMC2_WP	Write-Protect	PU10k

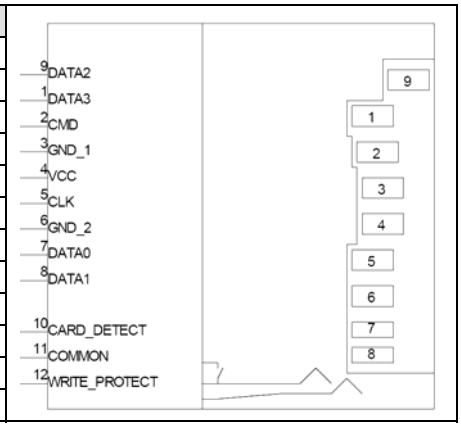


Table 29: Secure Digital / Multi-Media-Card X32

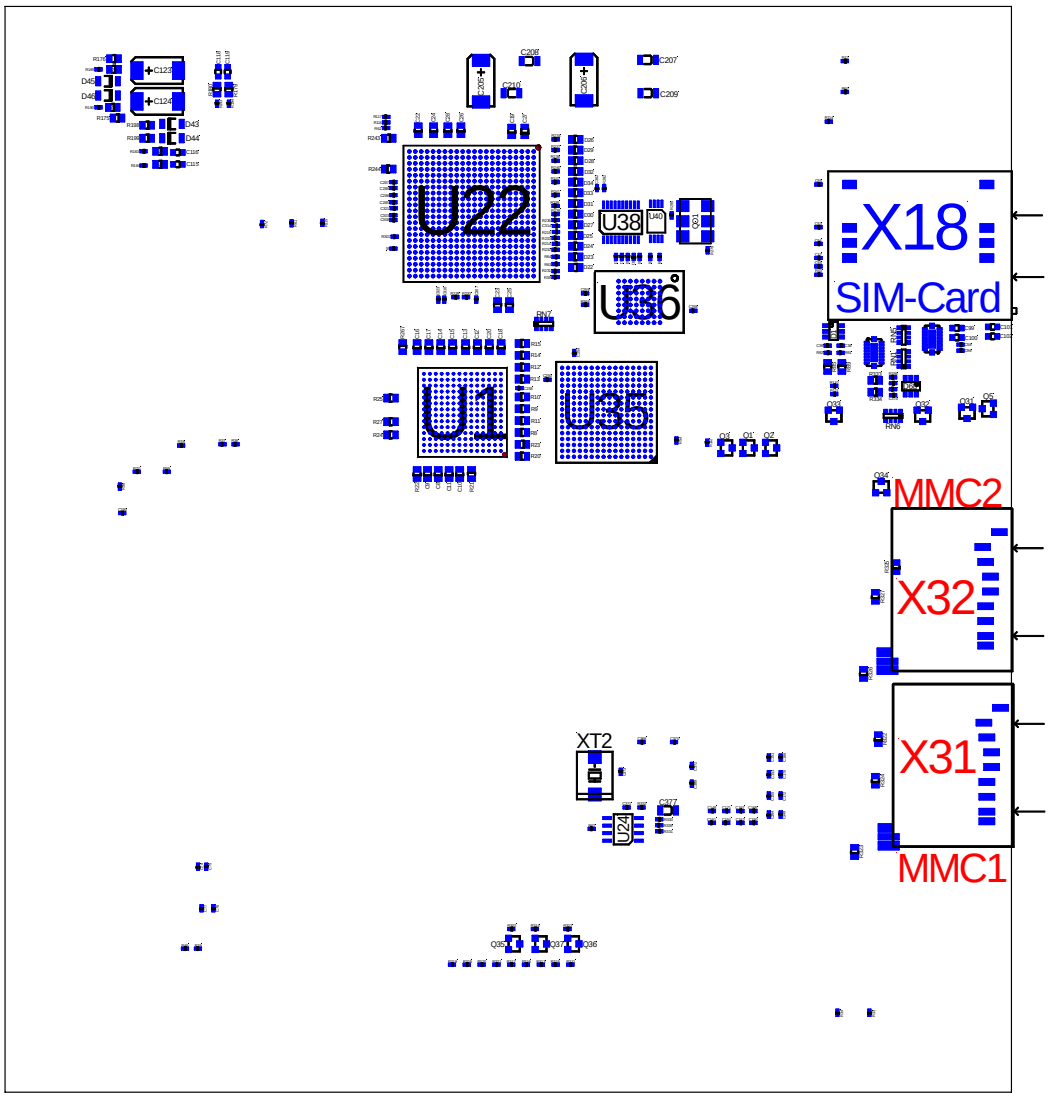


Figure 35: Secure Digital / Multi Media Card connector X30/X31

11.23 FPGA JTAG-pin header (X10)

Pin header X10 provides a connection to the baseboard FPGA JTAG-Port. The pinning is according Alteras recommendations. So it is possible to use an USB-Blaster etc. to program the ARIA-GX FPGA (U22).*Table 30* provides a detailed list of the signals found at X10.

Pin	Signal	Description	On-Board
1	ARIA_GX_TCK	JTAG TCK input	PD1K
2	GND	Ground	
3	ARIA_GX_TDO	JTAG TDO output	
4	VCC3V3S	Power	
5	ARIA_GX_TMS	JTAG TMS input	PU10K
6	VCC3V3S	Power	
7	N.C.		
8	N.C.		
9	ARIA_GX_TDI	JTAG TDI input	PU10K
10	GND	Ground	

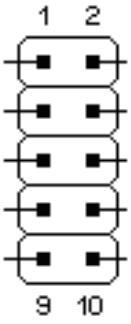


Table 30: FPGA JTAG pin header (X10)

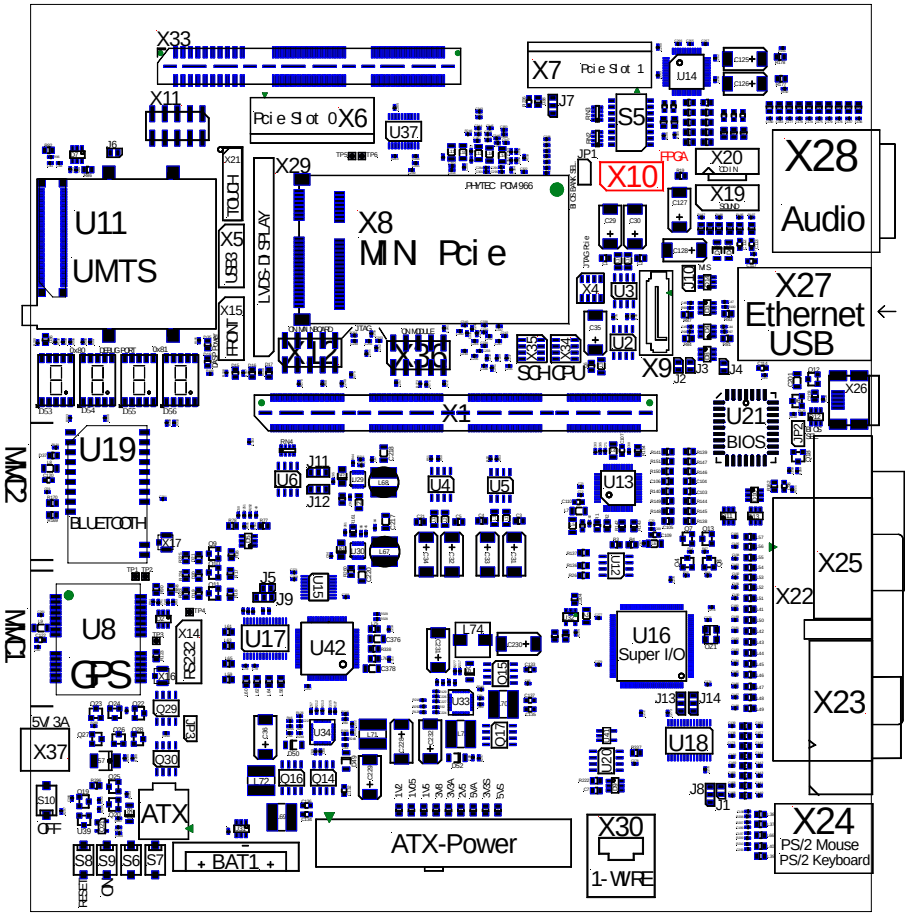


Figure 36: FPGA JTAG pin header X10

11.24 HSMA JTAG-pin header (X11)

Pin header X11 provides a connection to the HSMA JTAG-Port. The pinning is according Alteras recommendations. So it is possible to use an USB-Blaster etc. *Table 31* provides a detailed list of the signals found at X11.

Pin	Signal	Description	On Board
1	HSMA _TCK	JTAG TCK input	PD1K
2	GND	Ground	
3	HSMA_TDO	JTAG TDO output	
4	VCC3V3S	Power	
5	HSMA_TMS	JTAG TMS input	PU10K
6	VCC3V3S	Power	
7	N.C.		
8	N.C.		
9	HSMA_TDI	JTAG TDI input	PU10K
10	GND	Ground	

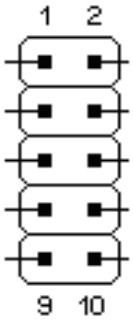


Table 31: HSMA JTAG pin header (X11)

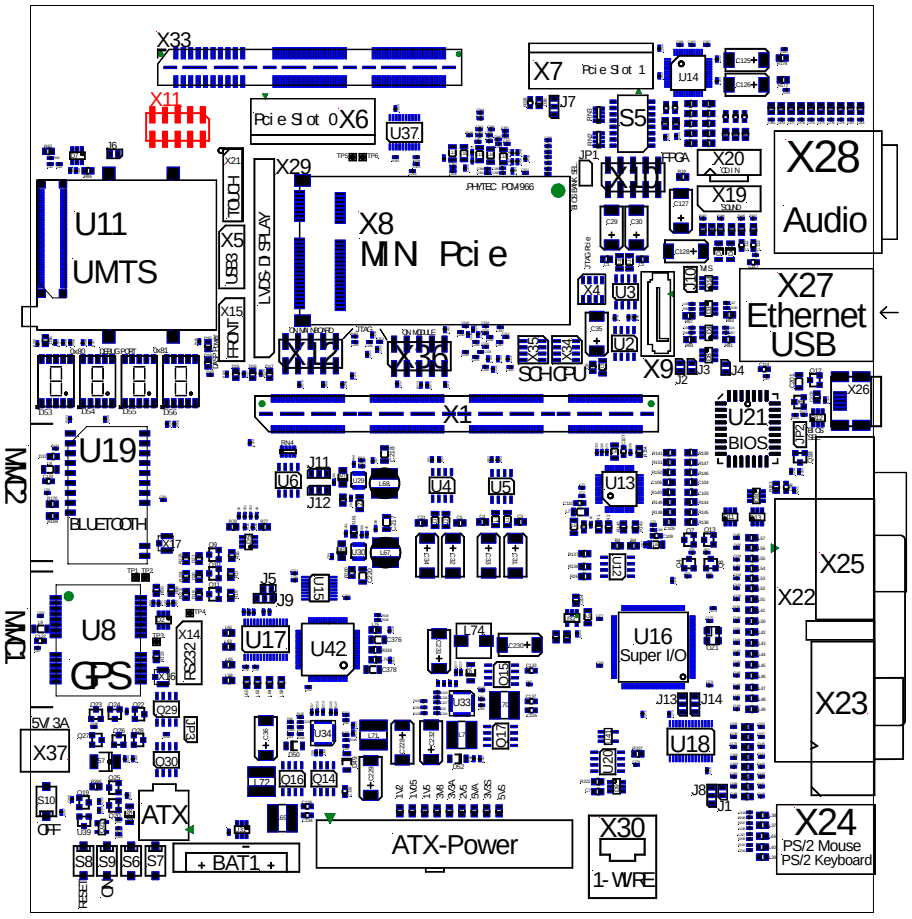


Figure 37: HSMA JTAG pin header X11

11.25 Baseboard PLD JTAG-pin header (X12)

Pin header X12 provides a connection to the baseboard PLD JTAG-Port. The pinning is according Alteras recommendations. So it is possible to use an USB-Blaster etc. *Table 32* provides a detailed list of the signals found at X12.

Pin	Signal	Description	On Board
1	PLD _JTAG_TCK	JTAG TCK input	PD1K
2	GND	Ground	
3	PLD_JTAG_TDO	JTAG TDO output	
4	VCC3V3S	Power	
5	PLD_JTAG_TMS	JTAG TMS input	PU10K
6	VCC3V3S	Power	
7	N.C.		
8	N.C.		
9	PLD_JTAG_TDI	JTAG TDI input	PU10K
10	GND	Ground	

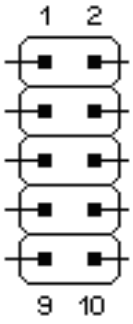


Table 32 PLD JTAG pin header (X12)

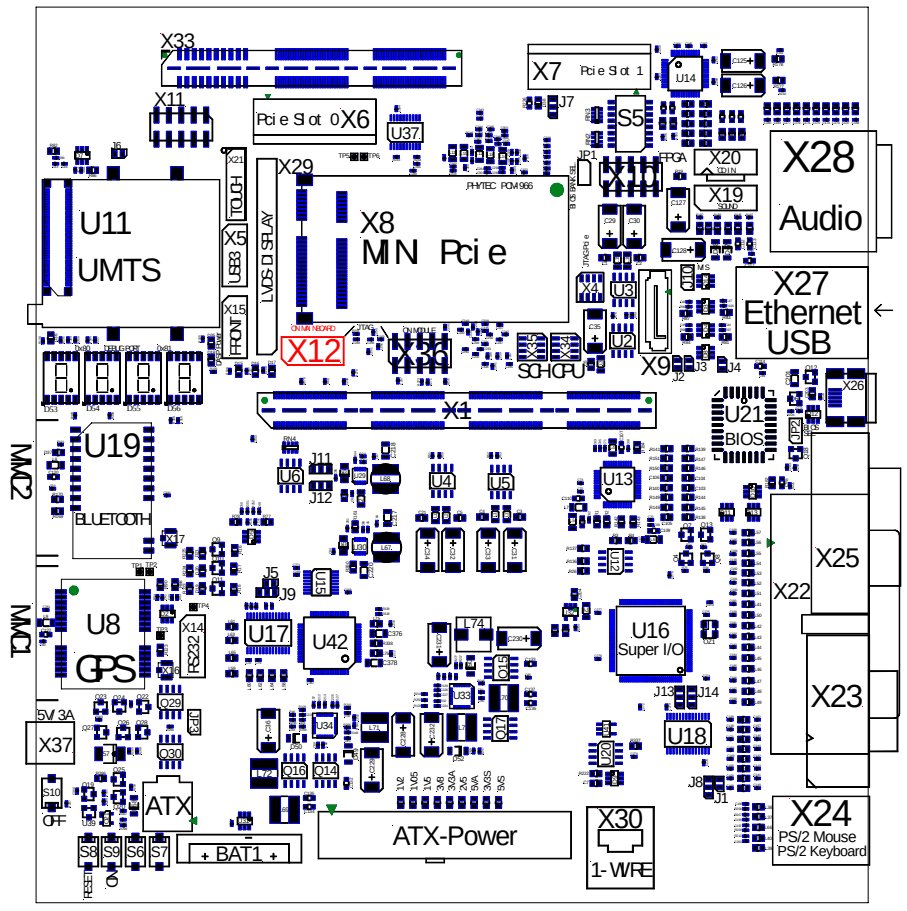


Figure 38: PLD JTAG pin header X12

11.26 PCIe-Switch JTAG-Port (X4)

The SMD connector X4 provides a connection to the baseboard PCIe switch 89HPES5T5 form IDT.*Table 33* provides a detailed list of the signals found at X4.

Pin	Signal	Description	On Board
1	VCC3V3S	Power	
2	JTAG_TDO_IDT	JTAG TDO output	
3	JTAG_TDI_IDT	JTAG TDI input	PU10K
4	N.C.		
5	JTAG_TRST_IDT	JTAG TRST input	PU10K
6	JTAG_TMS_IDT	JTAG TMS input	PU10K
7	GND	Power	
8	JTAG_TCK_IDT	JTAG TCK input	PD1K

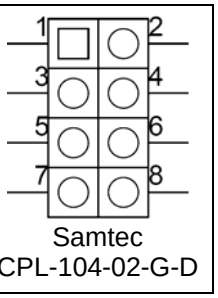


Table 33: PCIe Switch JTAG-Port (X4)

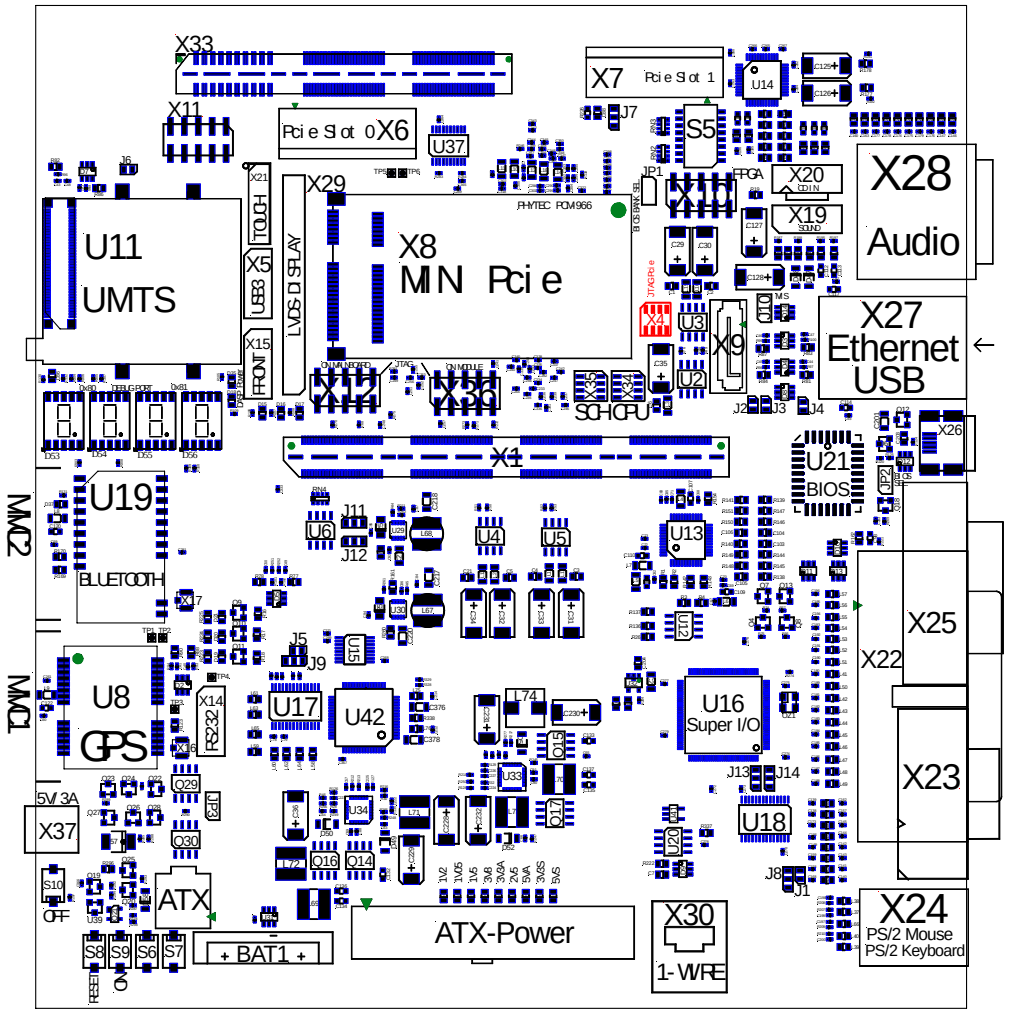


Figure 39: PCIe Switch JTAG-Port (X4)

11.27 Z500P(T) JTAG/XDP-Port (X34)

The SMD connector X34 provides a connection to the phyCORE-Z500P(T) CPU JTAG/XDP Port. Only the JTAG signals of the XDP Port are available at the phyCORE connector. *Table 33* provides a detailed list of the signals found at X34.

Pin	Signal	Description
1	VCC1V05S_JTAG	Power
2	XDP_TDO	JTAG TDO output
3	XDP_TDI	JTAG TDI input
4	N.C.	
5	#XDP_TRST	JTAG TRST input
6	XDP_TMS	JTAG TMS input
7	GND	Power
8	XDP_TCK_0	JTAG TCK input

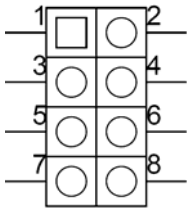


Table 34: Z500P(T) JTAG/XDP-Port (X34)

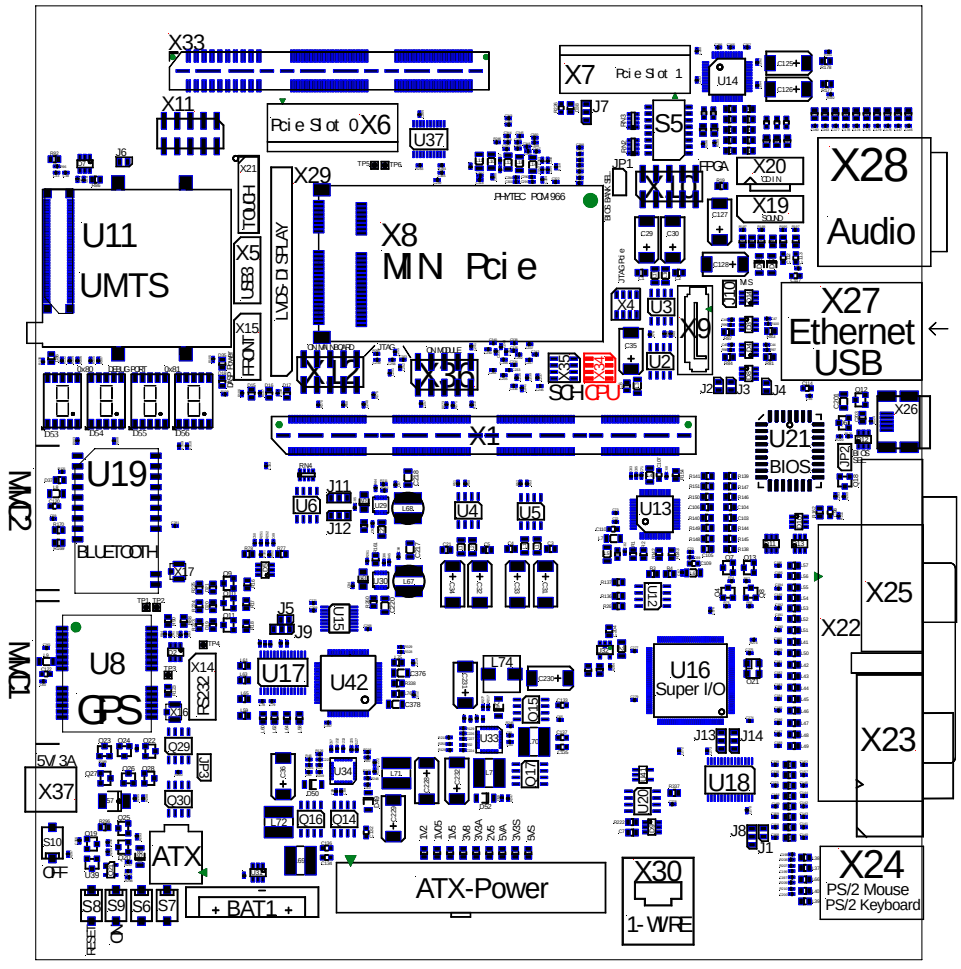


Figure 40: Z500P(T) JTAG/XDP-Port (X34)

11.28 US15WP(T) JTAG-Port (X35)

The SMD connector X35 provides a connection to the phyCORE-Z500P(T) SCH JTAG Port. *Table 35* provides a detailed list of the signals found at X34.

Pin	Signal	Description
1	VCC1V05S_JTAG	Power
2	SCH_TDO	JTAG TDO output
3	SCH_TDI	JTAG TDI input
4	N.C.	
5	#SCH_TRST	JTAG TRST input
6	SCH_TMS	JTAG TMS input
7	GND	Power
8	SCH_TCK	JTAG TCK input

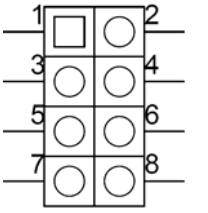


Table 35: US15WP(T) JTAG-Port (X35)

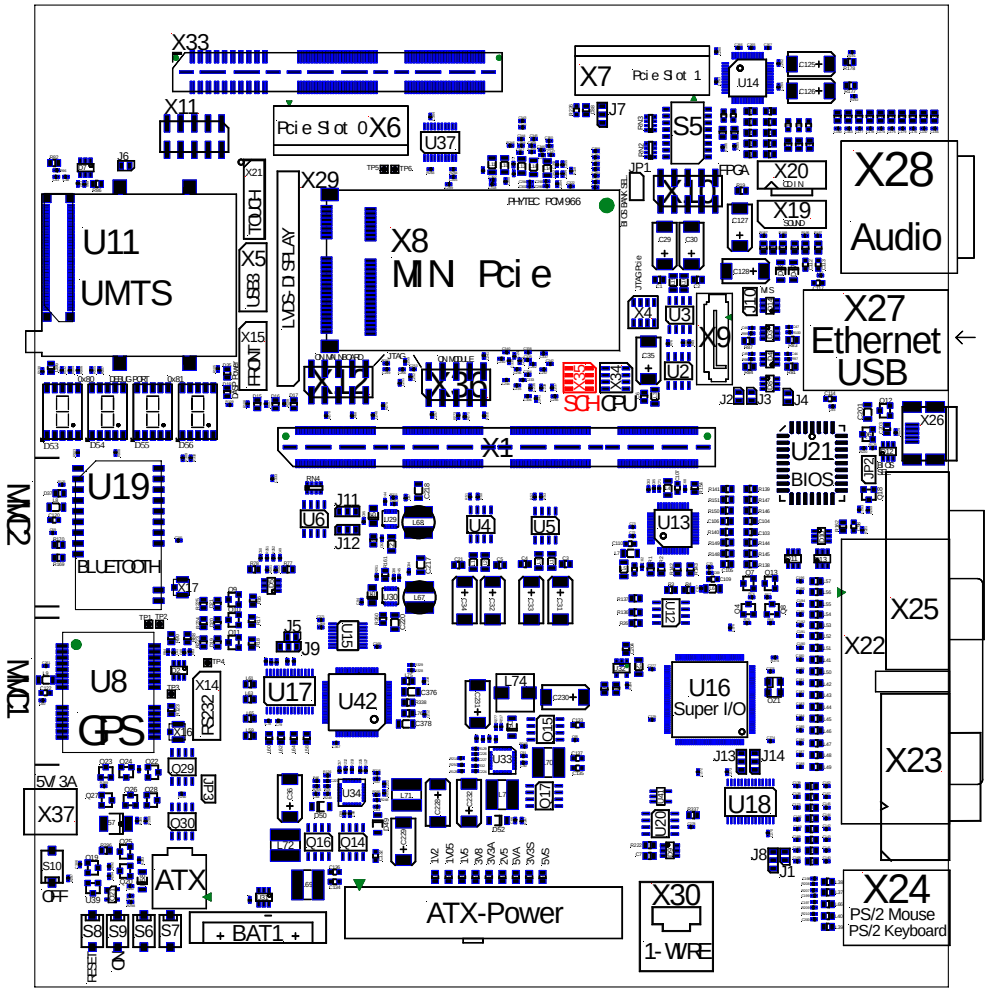


Figure 41: US15WP(T) JTAG-Port (X35)

11.29 phyCORE PLD JTAG-pin header (X36)

Pin header X36 provides a connection to the phyCORE PLD JTAG-Port. The pinning is according Alteras recommendations. So it is possible to use an USB-Blaster etc. *Table 36* provides a detailed list of the signals found at X36.

Pin	Signal	Description	On Board
1	PLD_TCK	JTAG TCK input	PD1K
2	GND	Ground	
3	PLD_TDO	JTAG TDO output	
4	VCC3V3S	Power	
5	PLD_TMS	JTAG TMS input	PU10K
6	VCC3V3S	Power	
7	N.C.		
8	N.C.		
9	PLD_TDI	JTAG TDI input	PU10K
10	GND	Ground	

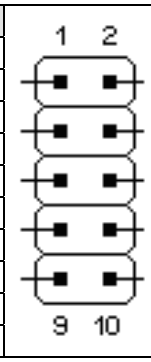


Table 36: phyCORE PLD JTAG pin header (X36)

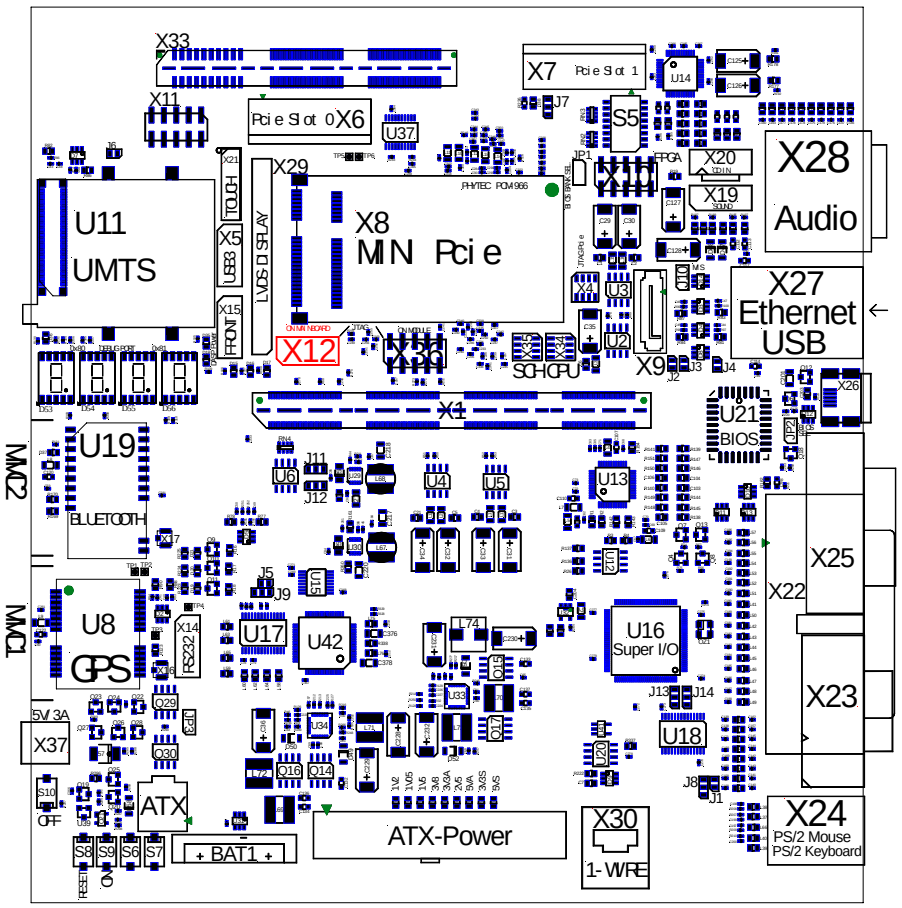


Figure 42: phyCORE PLD JTAG pin header X36

11.30 HSMC connector (X33)

The HSMC connector X33 provides a connection to the Aria-GX FPGA at the phyCORE-Z500P(T) baseboard. This connector follows the “High Speed Mezzanine Card (HSMC) Specification” from ALTERA. *Table 37*, *Table 38* and *Table 39* provide a detailed list of the signals found at X33.

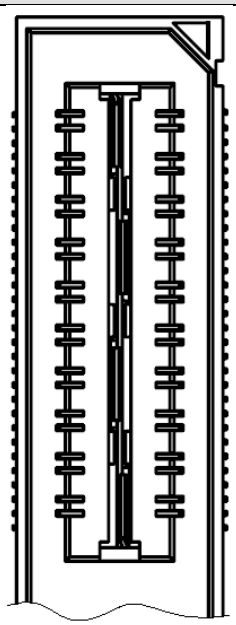
Pin	Signal	Bank 1	Signal	Pin
1	N.C.		N.C.	2
3	N.C.		N.C.	4
5	N.C.		N.C.	6
7	N.C.		N.C.	8
9	N.C.		N.C.	10
11	N.C.		N.C.	12
13	N.C.		N.C.	14
15	N.C.		N.C.	16
17	N.C.		N.C.	18
19	N.C.		N.C.	20
21	HSMA_TX_CP2		HSMA_RX_P2	22
23	HSMA_TX_CN2		HSMA_RX_N2	24
25	HSMA_TX_CP1		HSMA_RX_P1	26
27	HSMA_TX_CN1		HSMA_RX_N1	28
29	HSMA_TX_CP0		HSMA_RX_P0	30
31	HSMA_TX_CN0		HSMA_RX_N0	32
33	HSMA_SDA		HSMA_SCL	34
35	HSMA_JTAG_TCK		HSMA_JTAG_TMS	36
37	HSMA_JTAG_TDO		HSMA_JTAG_TDI	38
39	HSMA_CLK_OUT0		HSMA_CLKIN0	40

Table 37: HSMC connector X33 Bank 1

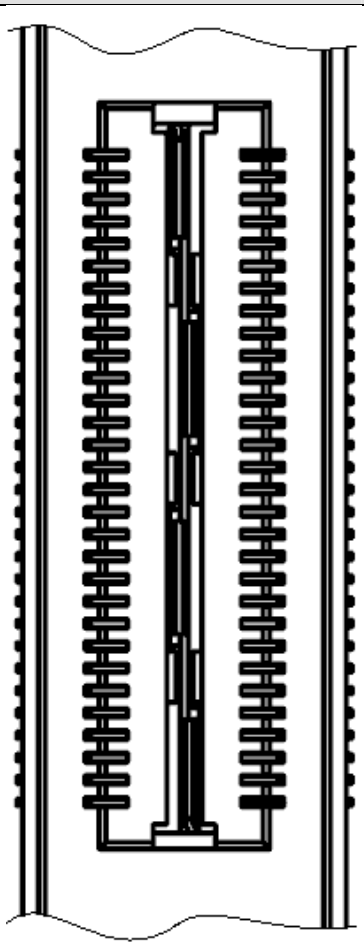
Pin	Signal	Bank 3	Signal	Pin
41	HSMA_D0		HSMA_D1	42
43	HSMA_D2		HSMA_D3	44
45	GND		GND	46
47	HSMA_TX_D_P0		HSMA_RX_D_P0	48
49	HSMA_TX_D_N0		HSMA_RX_D_N0	50
51	GND		GND	52
53	HSMA_TX_D_P1		HSMA_RX_D_P1	54
55	HSMA_TX_D_N1		HSMA_RX_D_N1	56
57	GND		GND	58
59	HSMA_TX_D_P2		HSMA_RX_D_P2	60
61	HSMA_TX_D_N2		HSMA_RX_D_N2	62
63	GND		GND	64
65	HSMA_TX_D_P3		HSMA_RX_D_P3	66
67	HSMA_TX_D_N3		HSMA_RX_D_N3	68
69	GND		GND	70
71	HSMA_TX_D_P4		HSMA_RX_D_P4	72
73	HSMA_TX_D_N4		HSMA_RX_D_N4	74
75	GND		GND	76
77	HSMA_TX_D_P5		HSMA_RX_D_P5	78
79	HSMA_TX_D_N5		HSMA_RX_D_N5	80
81	GND		GND	82
83	HSMA_TX_D_P6		HSMA_RX_D_P6	84
85	HSMA_TX_D_N6		HSMA_RX_D_N6	86
87	GND		GND	88
89	HSMA_TX_D_P7		HSMA_RX_D_P7	90
91	HSMA_TX_D_N7		HSMA_RX_D_N7	92
93	GND		GND	94
95	HSMA_CLK_OUT_P1		HSMA_CLK_IN_P1	96
97	HSMA_CLK_OUT_N1		HSMA_CLK_IN_N1	98
99	GND		GND	100

Table 38: HSMC connector X33 Bank 2

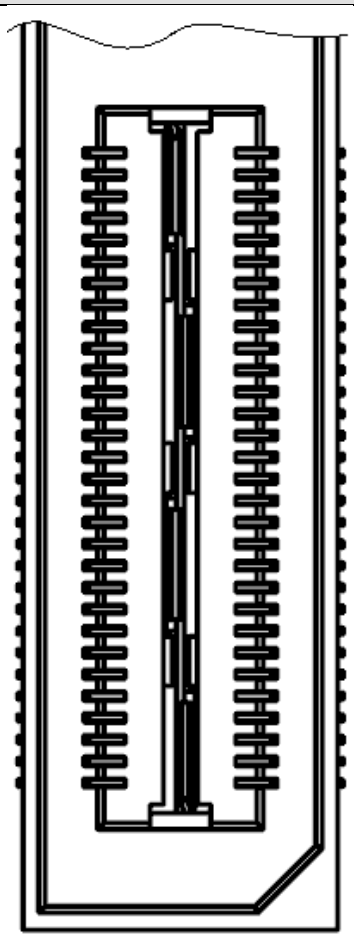
Pin	Signal	Bank 3	Signal	Pin
101	HSMA_TX_D_P8		HSMA_RX_D_P8	102
103	HSMA_TX_D_N8		HSMA_RX_D_N8	104
105	GND		GND	106
107	HSMA_TX_D_P9		HSMA_RX_D_P9	108
109	HSMA_TX_D_N9		HSMA_RX_D_N9	110
111	GND		GND	112
113	HSMA_TX_D_P10		HSMA_RX_D_P10	114
115	HSMA_TX_D_N10		HSMA_RX_D_N10	116
117	GND		GND	118
119	HSMA_TX_D_P11		HSMA_RX_D_P11	120
121	HSMA_TX_D_N11		HSMA_RX_D_N11	122
123	GND		GND	124
125	HSMA_TX_D_P12		HSMA_RX_D_P12	126
127	HSMA_TX_D_N12		HSMA_RX_D_N12	128
129	GND		GND	130
131	HSMA_TX_D_P13		HSMA_RX_D_P13	132
133	HSMA_TX_D_N13		HSMA_RX_D_N13	134
135	GND		GND	136
137	HSMA_TX_D_P14		HSMA_RX_D_P14	138
139	HSMA_TX_D_N14		HSMA_RX_D_N14	140
141	GND		GND	142
143	HSMA_TX_D_P15		HSMA_RX_D_P15	144
145	HSMA_TX_D_N15		HSMA_RX_D_N15	146
147	GND		GND	148
149	HSMA_TX_D_P16		HSMA_RX_D_P16	150
151	HSMA_TX_D_N16		HSMA_RX_D_N16	152
153	GND		GND	154
155	HSMA_CLK_OUT_P2		HSMA_CLK_IN_P2	156
157	HSMA_CLK_OUT_N2		HSMA_CLK_IN_N2	158
159	VCC3V3S		HSMA_PSINT	160

Table 39: HSMC connector X33 Bank 3

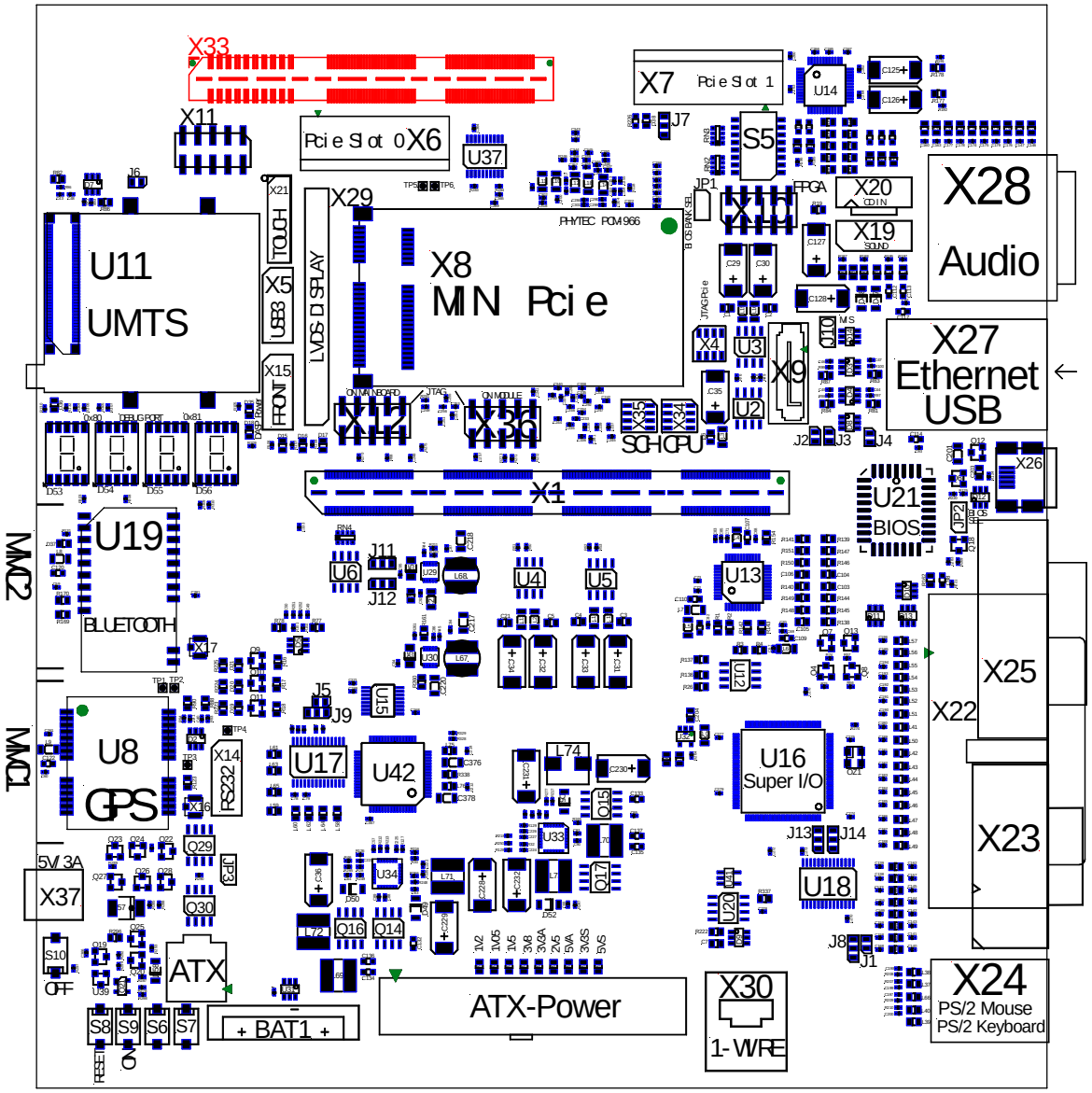


Figure 43: HSMC connector X33

11.31 PCIe at the phyCORE-Z500P(T) Baseboard

At the phyCORE-Z500P(T) are two PCIe x1 lanes available (if the Intel 82574 Ethernet is not populated). The second PCIe x 1 lane is connected to a 5-Lane 5 Port PCIe Switch to enable the user to use 2 PCIe x 1 and 1 miniPCEe card. The last PCIe x 1 lane is connected to the ARIA-GX FPGA.

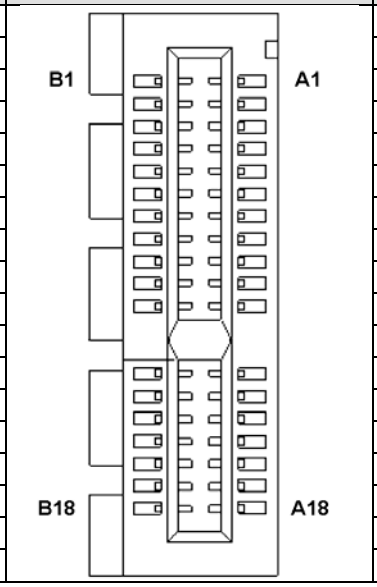
Pin	Signal		Signal	Pin
B1	ATX_12VDC		PCIE_SLOT0_PRESENT	A1
B2	ATX_12VDC		ATX_12VDC	A2
B3	N.C.		ATX_12VDC	A3
B4	GND		GND	A4
B5	SMB_CLK		N.C.	A5
B6	SMB_DATA		N.C.	A6
B7	GND		N.C.	A7
B8	VCC3V3S		N.C.	A8
B9	N.C.		VCC3V3S	A9
B10	VCC3V3A		VCC3V3S	A10
B11	#PCIE_WAKE		#RESET	A11
B12	N.C.		GND	A12
B13	GND		CLK_PCIE_SLOT4	A13
B14	PCIE_TXN_4		#CLK_PCIE_SLOT4	A14
B15	PCIE_TXP_4		GND	A15
B16	GND		PCIE_RXP_4	A16
B17	#CLK_PCIESLOT0_OE		PCIE_RXN_4	A17
B18	GND		GND	A18

Table 40: PCIe x 1 slot X6

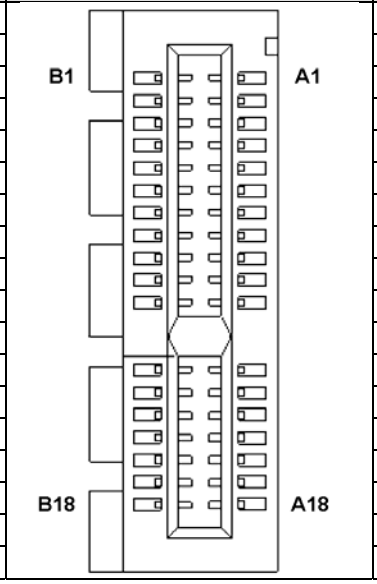
Pin	Signal		Signal	Pin
B1	ATX_12VDC		PCIE_SLOT5_PRESENT	A1
B2	ATX_12VDC		ATX_12VDC	A2
B3	N.C.		ATX_12VDC	A3
B4	GND		GND	A4
B5	SMB_CLK		N.C.	A5
B6	SMB_DATA		N.C.	A6
B7	GND		N.C.	A7
B8	VCC3V3S		N.C.	A8
B9	N.C.		VCC3V3S	A9
B10	VCC3V3A		VCC3V3S	A10
B11	#PCIE_WAKE		#RESET	A11
B12	N.C.		GND	A12
B13	GND		CLK_PCIE_SLOT5	A13
B14	PCIE_TXN_5		#CLK_PCIE_SLOT5	A14
B15	PCIE_TXP_5		GND	A15
B16	GND		PCIE_RXP_5	A16
B17	#CLK_PCIESLOT1_OE		PCIE_RXN_5	A17
B18	GND		GND	A18

Table 41: PCIe x 1 slot X7

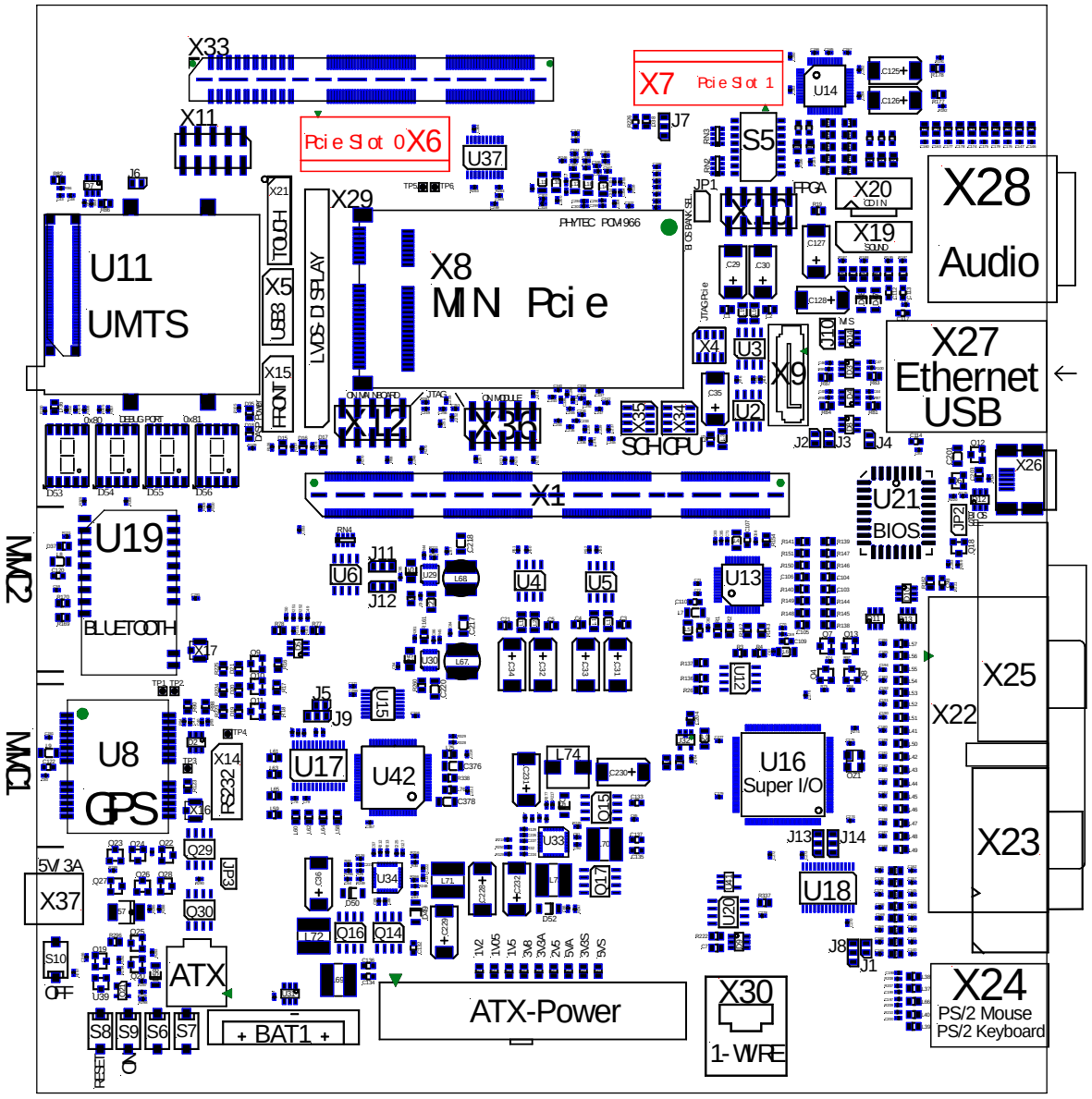


Figure 44: PCIe Slot X6/X7

11.32 PCIe mini Card Connector X8

The PCIe mini Card connector X8 provides the possibility to use mini PCIe cards at the phyCORE-Z500P(T) baseboard. *Table 42* provides a detailed list of the signals found at X8.

Pin	Signal		Signal	Pin
1	#PCIE_WAKE		VCC3V3S	2
3	N.C.		GND	4
5	N.C.		VCC1V5S	6
7	#CLK_MINIPCIE_OE		N.C.	8
9	GND		N.C.	10
11	#CLK_PCIE_SLOT6		N.C.	12
13	#CLK_PCIE_SLOT6		N.C.	14
15	GND		N.C.	16
17	N.C.		GND	18
19	N.C.		N.C.	20
21	GND		#RESET	22
23	PCIE_RXN_6		VCC3V3A	24
25	PCIE_RXP_6		GND	26
27	GND		VCC1V5S	28
29	GND		SMB_CLK	30
31	PCIE_TXN_6		SMB_DATA	32
33	PCIE_TXP_6		GND	34
35	GND		USB_DN_3_CON	36
37	N.C.		USB_DP_3_CON	38
39	N.C.		GND	40
41	N.C.		Led D15	42
43	N.C.		Led D16	44
45	N.C.		Led D17	46
47	N.C.		VCC1V5S	48
49	N.C.		GND	50
51	N.C.		VCC3V3S	52

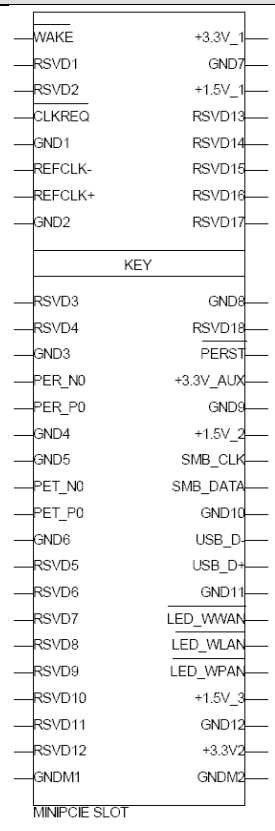


Table 42: miniPCIe slot X8

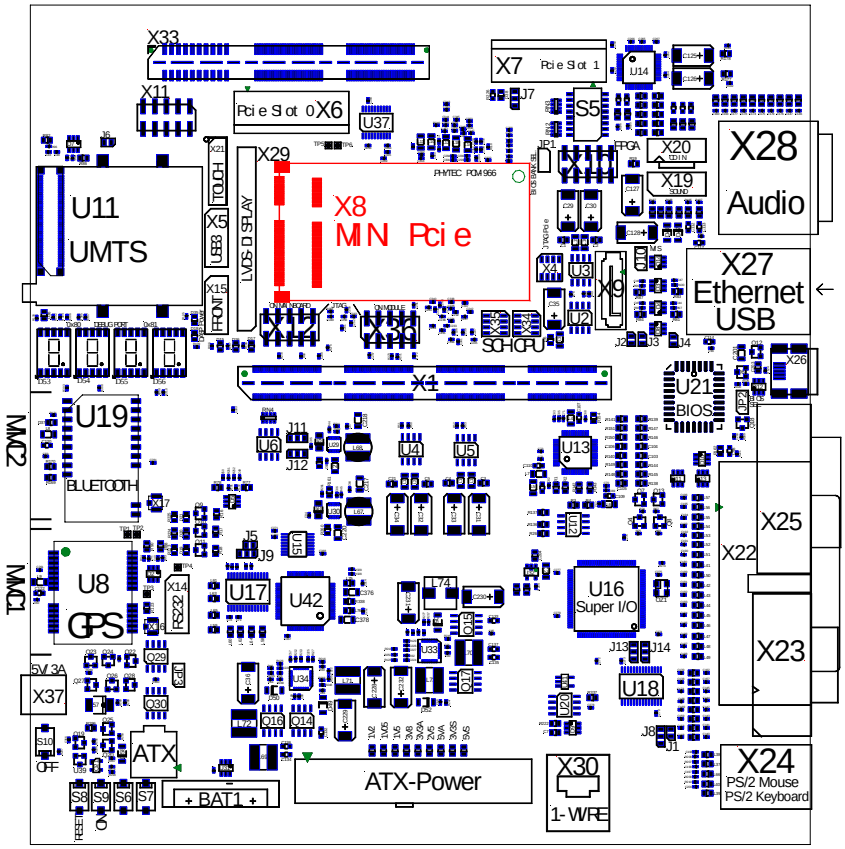
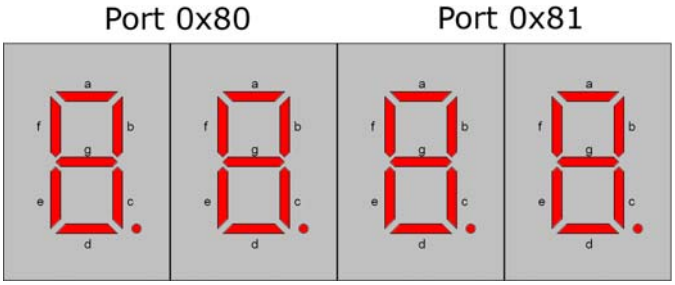


Figure 45: PCI Express Mini Card connector X8

11.33 Post Code Display / Debug-Port 0x80,0x81

To simplify debugging of software, two 8-Bit display ports are available at the phyCORE-Z500P(T) baseboard. They are write accessible via I/O-Address 0x80 and 0x81.



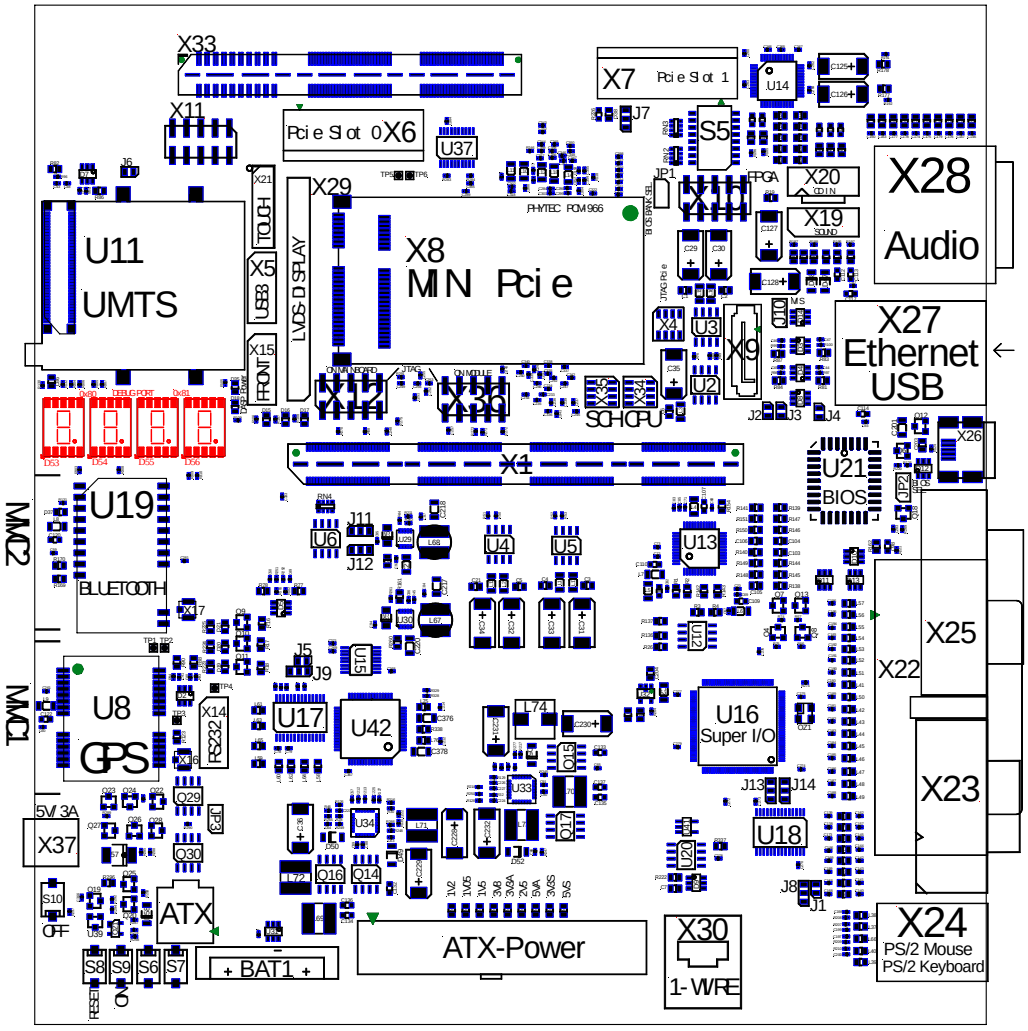


Figure 46: Debug Port 0x80/0x81

11.34 Push Buttons and LEDs

The phyCORE-Z500P(T) baseboard provides a variety of buttons and LEDs for input, feedback, and status purposes. A detailed description of each button and LED is presented in below.

LED	Signal	Description
D15	#LED_WPAN	PCIe mini Card WPAN status
D16	#LED_WLAN	PCIe mini Card WLAN status
D17	#LED_WWAN	PCIe mini Card WWAN status
D18	DASP	Drive activity (SDD/SATA)
D19	MMC2_LED	Multimedia Card slot 2 activity
D20	MMC1_LED	Multimedia Card slot 1 activity
D21	MMC0_LED	Multimedia Card slot 0 activity
D35	Power	General Power LED
D36	UMTS	UMTS status display
D37	Bluetooth	Bluetooth activity
D59	1V2	1V2 Voltage regulator
D60	1V05	1V05 Voltage regulator
D61	1V5	1V5 Voltage regulator
D62	3V8	3V8 Voltage regulator
D63	3V3A	3V3A Voltage regulator
D64	2V5	2V5 Voltage regulator
D65	5VA	5VA Voltage regulator
D66	3V3S	3V3S Voltage regulator
D67	5VS	5VS Voltage regulator

Table 43: LEDs at the baseboard

Switch	Signal	Description
S6	USER_PB0	General User Button connected to the FPGA
S7	USER_PB1	General User Button connected to the FPGA
S8	#PM_SYSRST	System reset
S9	#PWR_BTN	Power
S10	Power Off	Hard power off

Table 44: Switches at the baseboard

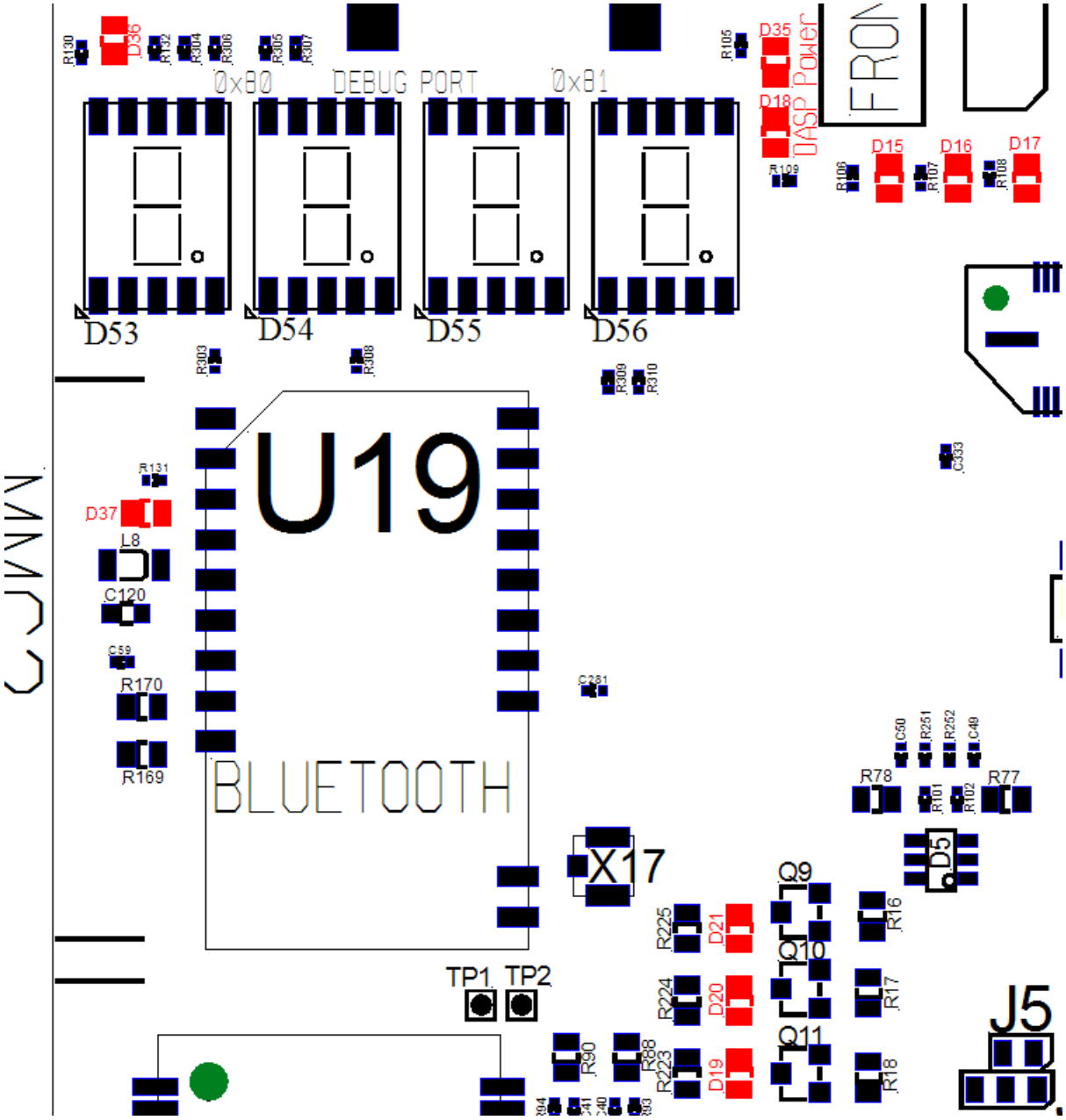


Figure 47: Push Buttons and LEDs

11.35 Address-Map / USB-Tree

I/O-Addresses	Name	Description	Location
0x800	SPISEL	Read/write to the SPI-Flash with activating /CS	phyCORE
0x801	SPIDSEL	Read/write to the SPI-Flash with deactivating /CS	phyCORE
0x80	Debug Port 0x80	Write only Debug Port	Baseboard
0x81	Debug Port 0x80	Write only Debug Port	Baseboard
0x378	LPT	Printer-Port (IRQ-5)	Baseboard Super-IO
0x3f8	COM1	Serial Port 1 (IRQ4)	Baseboard Super-IO
0x2f8	COM2	Serial Port 2 (IRQ3)	Baseboard Super-IO

Table 45: I/O-Address Map

I²C-Addresses	Description	Location
0xA0	SPD EEPROM (U8)	phyCORE
TBD	SMB Interface of 82574L (U16)	phyCORE
0xD2	SMB Interface of Clock Chip ICS9UM633 (U26)	phyCORE
0xEE	Slave Interface of PCIe switch 89HPES5T5 (U1)	Baseboard
0xBE	Master Interface of PCIe switch 89HPES5T5 (U1)	Baseboard
Unknown	SMB Interface of GPS chip LEA-5H	Baseboard

Table 46: I²C-Address Map (8-bit)

USB-Port	ID	Description
0	---	Low-/Full-/High-Speed Host at X27
1	---	Low-/Full-/High-Speed Host at X27
2	---	Low-/Full-/High-Speed Client or Host at X26
3	---	Low-/Full-/High-Speed Host Universal LVDS interface X29 / USB-Header X5
4	1bc7:1003	GSM/UMTS Module U11 at full speed
5	1546:01a5	Full speed Interface of GPS chip LEA-5H
6		ONLY High-Speed Host at X5
7	0403:6011	ONLY High-Speed to Quad FTDI U42

Table 47: USB Port usage

11.36 Baseboard Physical Dimension

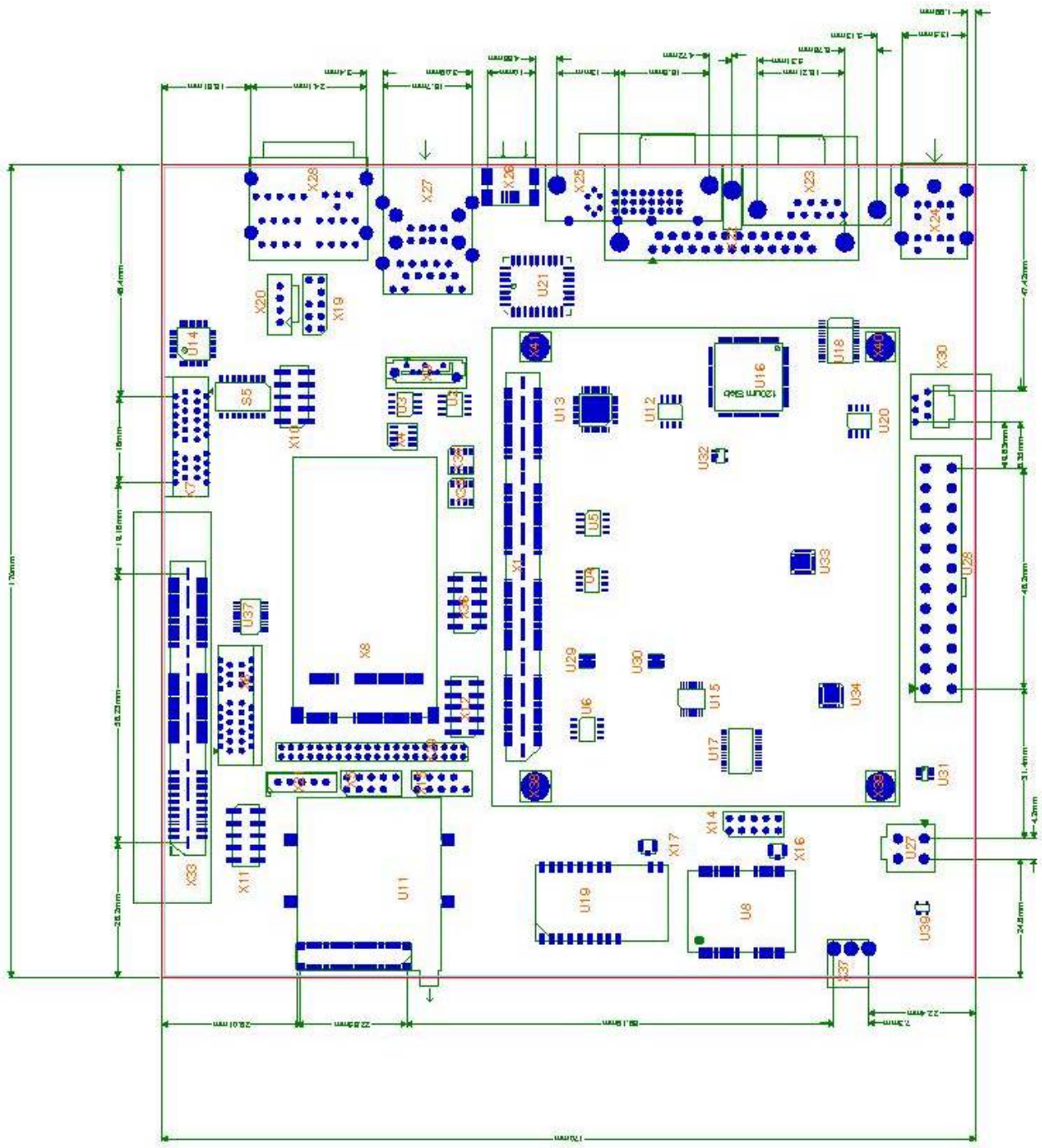


Figure 48: Baseboard physical dimensions

12 Revision History

Date	Version numbers	Changes in this manual
02-July-2009	Manual L-732e_0 PCM-041 PCB# 1310.1 PCM-966 PCB# 1312.1	First draft, Preliminary documentation. Describes the phyCORE-Z500P(T) with phyCORE-Z500P(T) Baseboard.

13 Component Placement Diagram

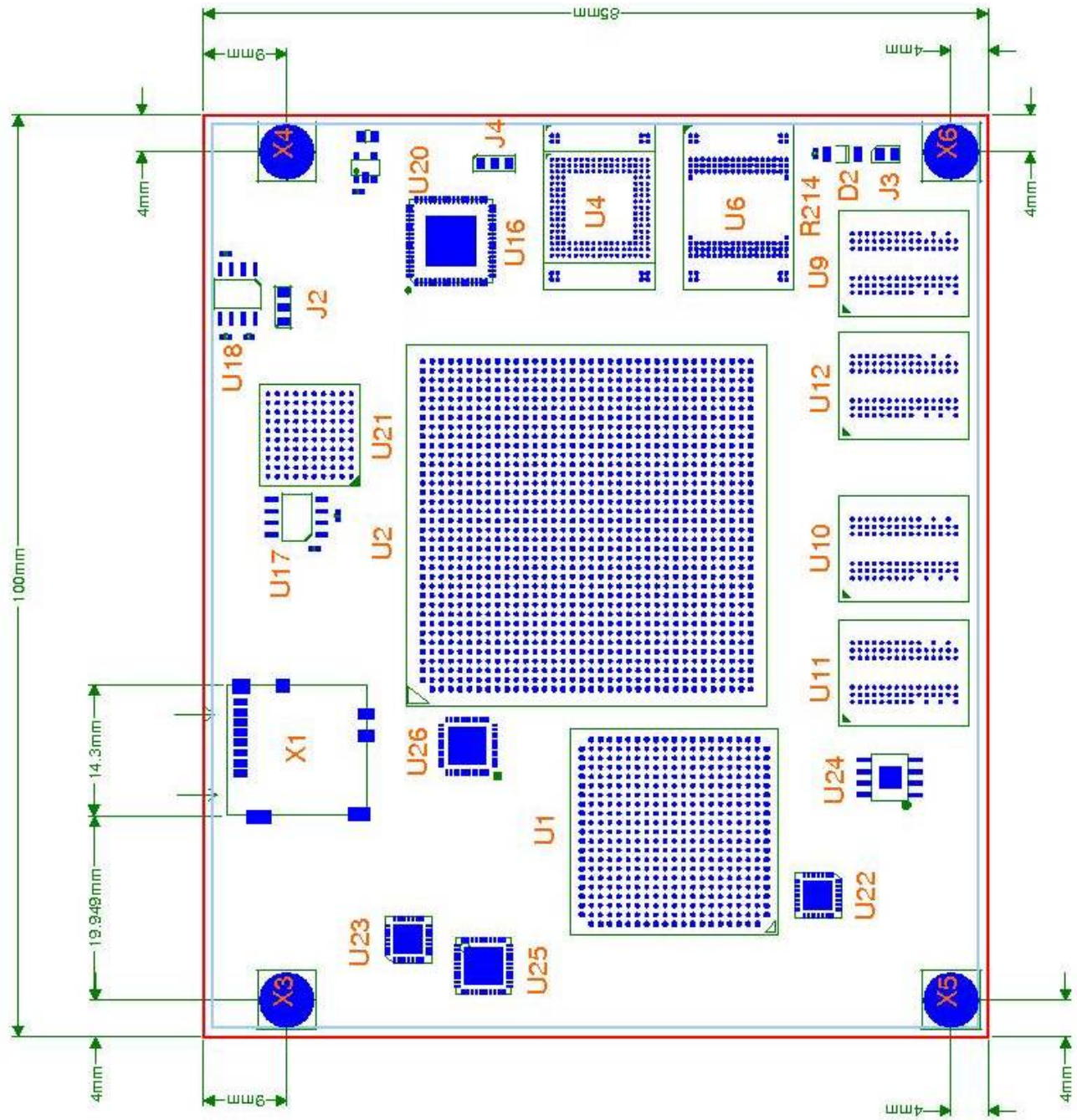


Figure 49: phyCORE-Z500P(T) Component Placement, Top View

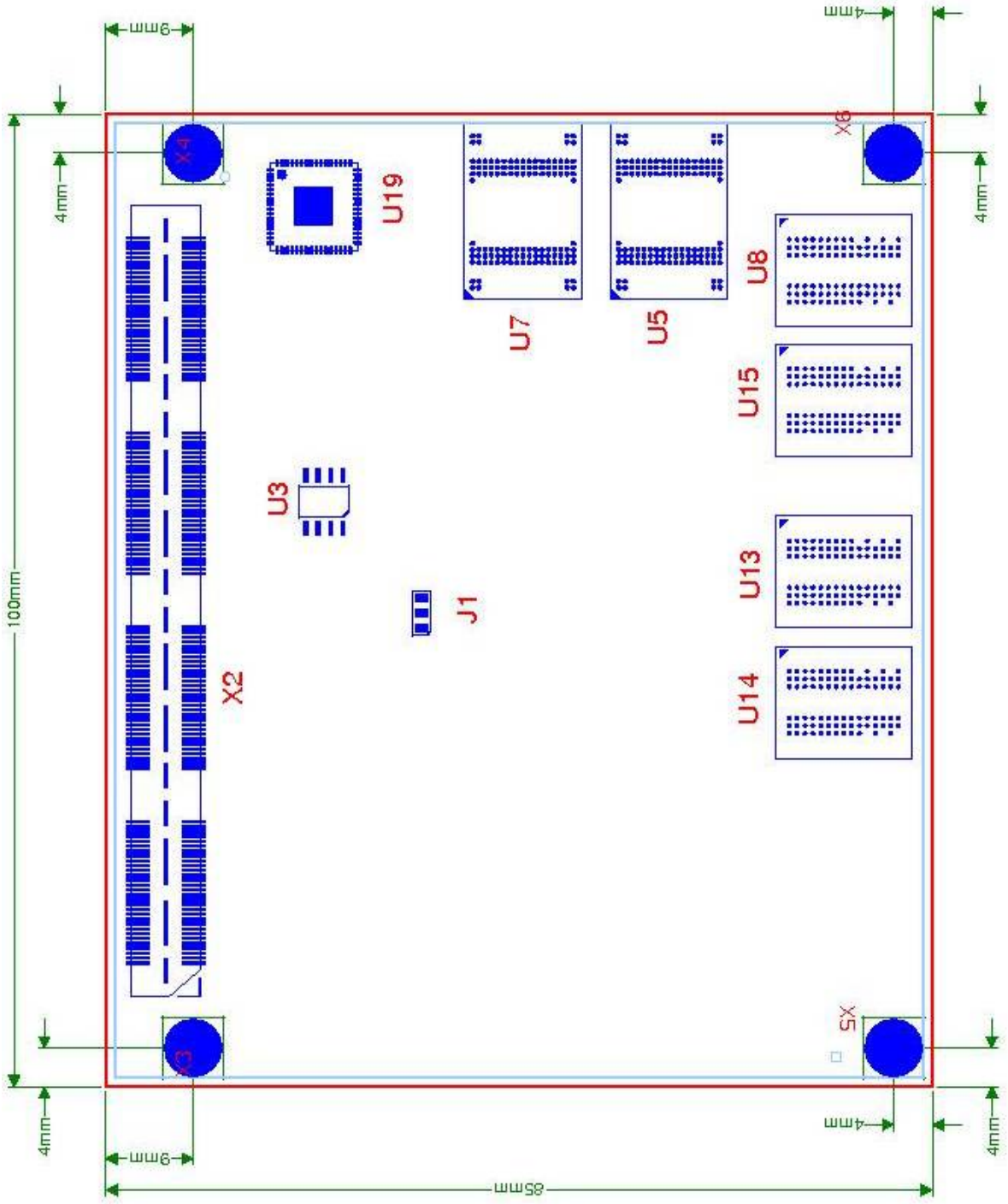


Figure 50: phyCORE-Z500P(T) Component Placement, Bottom View

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Document:	**phyCORE-Z500P(T)**
Document number:	**L-732e_0, Preliminary Version, July 2009**

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