PHYTEC

miniMODUL-537

Hardware Manual

Edition November 1993

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Information for the miniMODUL-537

For the standard Version of this module with EPROM from 0000H (plain Monitor-Mode or user machine program) the diode besides JP2/JP7 at the bottom side of the circuit board should not be installed.

This is only required in combination with our Monitor-Basic. To make possible a change of the module, this diode is soldered only at one end for a redesign of the layout, except if there are no demands from you otherwise.

Therefore there is no defect of our product because the diode is soldered only at one end.

1 Introduction

The miniMODUL-537 from PHYTEC is a universal microcontroller board of credit-card size for applications in measuring and Control Engineering.

The miniMODUL-537 with the microcontroller SAB80C537 is an additional member of the credit-card size minicomputer series from PHYTEC. The predecessors of this product are the miniMODUL-535 with the SAB80C535 microcontroller from Infineon and the miniMODUL-552 with the microcontroller 80C552 from VALVO/PHILIPS. All controllers are based on the architecture of the 8051 microcontroller family and have in general compatible instruction sets. As developing tools, all assembler and compiler for the 8051-family can be applied.

All those processors contain considerable extensions of the integrated peripherals as there are interfaces, timer, A/D converter and parallel ports. The external components like RAM, ROM, Real-Time Clock, decoder, battery back-up and monitor are already available on the miniMODUL-537 with modern SMD technique.

The miniMODUL-537 is a complete microprocessor-system with versatile peripheral functions, and the necessity to develop a digital microprocessor system for the application hardware can be avoided. The miniMODUL-537 is plugged on to the application hardware, which might be not very extensive, like a “big chip”.

The favorable cost-performance ratio liberates you from development, design and test of a digital system.

For the 8051-family various assembler and compiler are available on the market. PHYTEC offers for simple programming of the module a Basic-interpreter and a monitor program. In the simplest instance only a terminal is required, since the interface drivers are already implemented. With the help of a PC the up/downloading of programs is possible during the test phase. In combination of user PC-software with C51, A51 and DSCOPE51 efficient program developing is possible.

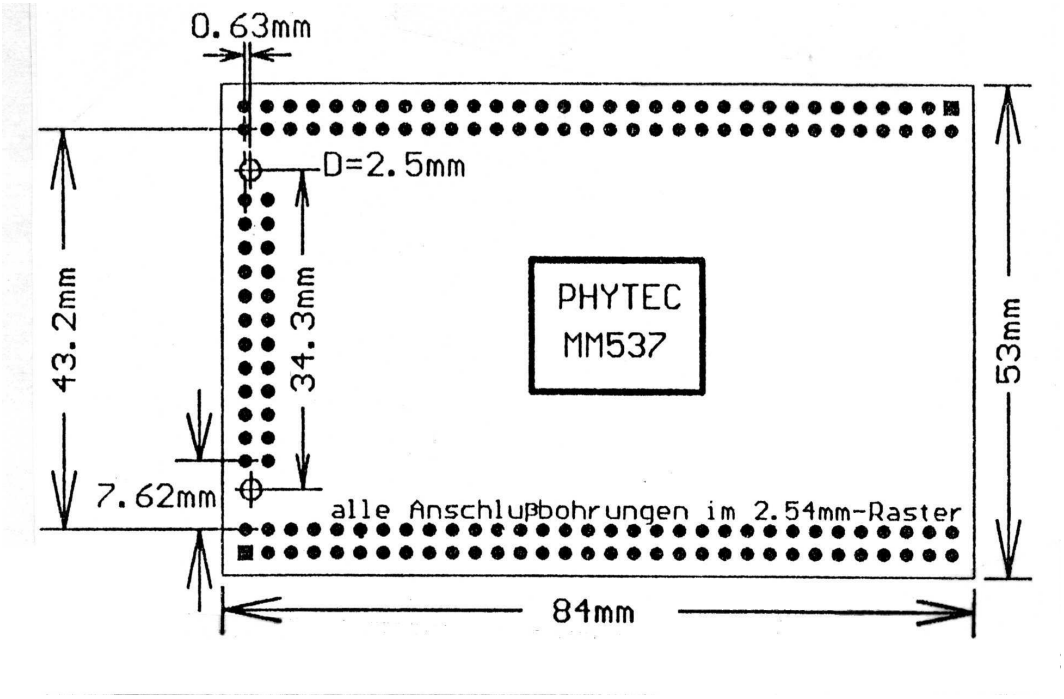

Figure 1: Dimensions of the miniMODUL-537

2 Installation and Setting into Operation

The miniMODUL-537 requires a stabilized supply voltage of 5 V. The current consumption is less 100 mA. Please employ only reliable voltage regulators (for example 7805), since overvoltages might be produced by bad power supplies or laboratory power supplies with adjustable voltage, and damage the module. The connections of the supply voltage are found in diagonal corners of the module. The printing on the board designates GND with '-' and VCC with '+'.

The following pins are connected to VCC or GND:

A1, A2, B1, B2 - VCC
A63, A64, B63, B64 - GND

The connection of one point is sufficient for example VCC to A1 and GND to B1.

The supply voltage should not decrease below 4.8 V. Otherwise a reset might automatically be triggered, which stops all operations. In case of problems, check if the supply voltage is to low. Also short voltage fluctuations have to be considered.

2.1 The Serial Interface

If an EPROM was installed by the manufacturer, usually all jumpers are configured properly. In order to communicate with our Monitor-program or Monitor-Basic, the connections of the RS-232 interface A45, A47 with a terminal or PC/AT are required. Those programs don't use handshake-lines, since they are operating with XON/XOFF protocol. Connect the RS-232-input A45 with the RS-232-output of your PC/AT or terminal and the RS-232-output A47 with the corresponding input of the terminal or PC/AT. The standard RS-232 connection is especially designated on the printing of the circuit board. The arrows symbolize the flow of the signals. **Don't forget the GND-connection for example to A63**.

The standard baud rate is 9600 baud. The transmission format is 8 data bit, no parity, one start bit and one stop bit.

In case of malfunctioning, check if RxD and TxD are exchanged. With a usual voltage meter you can measure, if at the TxD-connection a negative voltage between –7 V ..-12 V against GND is found. RxD has a voltage of 0 V against GND.
Please connect always TxD with RxD and RxD with TxD. If sometimes the transmission is failing, the GND-line might be connected in the wrong way.

2.2 The RESET

The RESET is activated automatically at turn on. For an unfavorable increase of the supply voltage eventually a manual RESET might be required. Trigger this RESET by shorting the adjacent connections A61 (/RESIN) and A63 (GND). Please maintain this connection for at least half a second. The manual RESET doesn't produce a continuous-RESET, but equidistant RESET-pulses. A continuous-RESET is achieved by the connection of A34 with GND. The connection should not be bouncing. In order to recognize the connections easily, A61 and A63 are signed with a square.

2.3 The PC/AT Communication-Program

Your PC/AT doesn't notify the RS-232-interface, as long as no corresponding program is started.
In order to display data from the miniMODUL-537 and to enter data via the RS-232 interface, a communication program has to be started on a PC/AT. Therefore we include the program MONTERM in the software package of Monitor and Monitor-Basic. The invocation of this program is achieved by the following command:

```
MT <cr>                          ; for 9600 baud
MT BAUDRATE (19200) <cr>         ;for other baud rates (19200 baud)
```

After the start of MONTERM and a RESET of the miniMODUL-537 the message of the installed software should be displayed on the screen.

2.4 Malfunctioning of the PC/AT

For the utilization of other PC-communication-programs as MONTERM we don't guarantee proper operation.

The miniMODUL-537 is only malfunctioning, if despite correct jumper setting and with our standard EPROMs no output can be observed at TxD of the miniMODUL-537 after a RESET. In case of problems, check the signal with an oscilloscope at point A47.

The reason for no operation might be either a bad cable or PC-interface or PC-software. A simple method to check the operation of the PC is to connect TxD and RxD of the PC before the miniMODUL-537 was separated. Actuation of a key at the PC will result in the echo of this key displayed at the screen of the PC.

2.5 Installation of User-Programs on the miniMODUL-537

When installing user-programs on the module, pay attention to the correct configuration of the jumpers, which are mostly found on the back-side of the module. Those jumpers select the address regions, the access mode and the chip-type for RAM, EPROM and eventually EEPROM. Select the jumpers according to the description found in *section 5.* The serial interfaces with RS-232 and RS-485 standard are already connected from the controller to the corresponding ports. If the port pins should be used for other purposes those conductor stripes have to be cut. More detailed information of the serial interfaces is found in *section 6.*

3 Pin Configuration

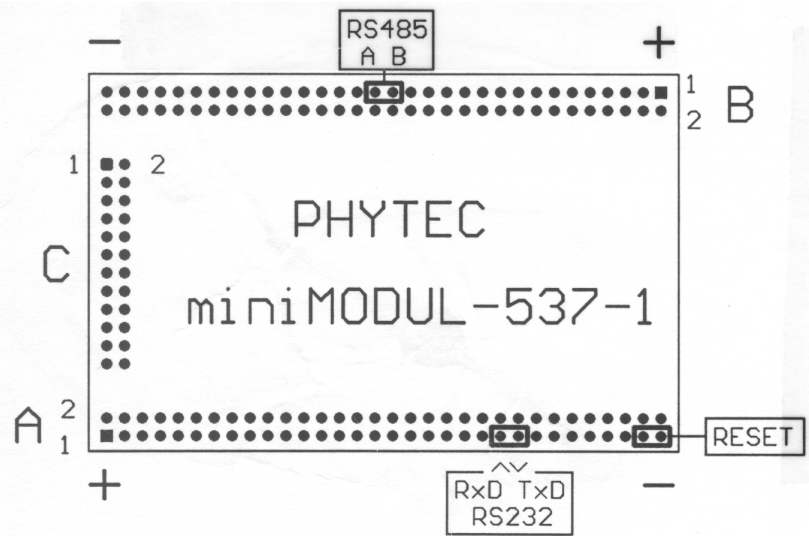

Figure 2: Pin Connection

The miniMODUL-537 has two connecting strips A and B with 64 connections each. Here all connections for supply voltages, digital signals and some control-lines are found. The analog-inputs and reference voltages are positioned in the connecting stripe C. The pins with uneven number are at the outside and the pins with even number are at the inside.

The supply voltages GND and VCC are applied in diagonal on two corners of the board. The printing on the board designates VCC by '+' and GND by '-'. For uncritical applications, VCC and GND have to be connected only once.

All signals with few exceptions are positioned efficiently and packed analog to their function in the connection stripe. The printing on the board shows lines to indicate the different functions and help to recognize the proper connections of the ports. Bit 0 is signed with a point '.'. For detailed positioning of the remaining signals use the pin assignment diagram.

Often used connections, like the serial interface 0, the RESET-input and the RS-485-connections are especially signed with a quadrangle

The connections in detail

In the following, connections with the supplement 'TTL' have TTL level, but must not coincide in every respect to the TTL standard. Notice, that the parallel ports have a characteristic output curve, which differs from TTL-outputs. More information is found on page 61 of the controller manual.

The supply voltage

A1, 2 and B1, 2	Supply voltage VCC of 5.0 V	
A63,64 and B63,64	Digital Ground	
A42	Battery voltage input	3 V
A32	Battery voltage output	3 V/ 5 V
C01..C21	Analog-GND VAGND	
C23	Analog-reference voltage VAREF	

Data-address bus

More detailed information of the performance, loading capacity and DC-characteristic can be depicted from the INFINEON controller manual of the SAB80C537, starting on page 61 and 336 respectively.

B10..B03	D0..D7	Data bus
B18..B11	A0..A7	Address bus low
B19,..,B26	A8..A15	Address bus high Attention counting!

The general controller ports

More detailed information of the performance, loading capacity and DC-characteristic can be depicted from the INFINEON controller manual of the SAB80C537, starting on page 61 and 336 respectively.

A30..A23 Port 1 (Ext. interrupts, timer 2-control)
A15..A22 Port 3 (Ext. int., timer 0/1-control, SERIAL0,/RD,/WR)
A03..A10 Port 4 (Compare-unit)

B52..B45 Port 5 (Concurrent-compare-unit)
B55..B62 Port 6 (AD-converter, SERIAL 1)

C10..C24 Port 7 (Analog-inputs AN00..AN07)
C02..C08 Port 8 (Analog-inputs AN08..AN10)

The exact pin assignment of the ports and their alternative functions are described in the controller manual page 68 and the corresponding sections.

Decoder-Control-Signals

The decoder-control-signals are only relevant in case an external decoder is connected, which replaces the module-internal minimum decoder.

B42 XROM ROM Decoder-selection

Input: open if no external address decoder to /XOEROM and /XCEROM should be connected. Status LOW switches off the module internal selection of the EPROM U11.

B41 /XOEROM ROM Output_Enable

Input/Output active LOW. Can be connected to an external address decoder. For this purpose XROM must be connected permanently or temporarily to LOW.

A58 ROM A15 ROM A15

Input: Can be wired from outside for special purposes. Then jumper JP9 must be open.

B38 XRAM2 RAM 2 (U12)-Decoder selection

Input: Open, if no external address decoder should be connected to /XCERAM2. Status LOW switches off the modules internal selection of RAM U12.

B37 /XCERAM2RAM 2 (U12) Chip-Enable

Input/Output active LOW. Can be connected to an external address decoder. For this purpose XRAM2 must be connected permanently or temporarily to LOW.

B40 XRAM1 RAM 1 (U13)-Decoder selection

Input: Open, if no external address decoder should be connected to /XCERAM1. Status LOW switches off the module internal selection of RAM U13.

B39 /XCERAM1RAM 1 (U13) Chip-Enable

Input/Output active LOW. Can be connected to an external address decoder. For this purpose XRAM1 has to be connected permanently or temporarily to LOW.

B43 XCEROM

Input/Output active LOW. Can be connected to an external address decoder. For this purpose XROM has to be connected permanently or temporarily to LOW.

Clock-Control-signals

A60 STDP Standardpulse of the optional Real-Time Clock

Output active LOW. Pulse 1/60 sec cycle, second cycle, minute cycle or hour cycle. More information are taken from the data sheet *section 11* of the Real-Time Clock.

A59 /CSRTC Chip-Enable of the optional Real-Time Clock

Input active LOW. Can be connected with a vacant controller port or an external address decoder.

RS-232-Driver connections

A47 T10 TxD 0 (Transmitter 1 Output)

Output for RS-232 for the serial interface SERIAL 0 of the SAB80C537.

A41 T1I Transmitter 1 Input

Input: Already connected to TxD0 of the controller. For other utilization, cut the connection with TxD0.

A45 R1I RxD 0 (Receiver 1 Input)

Input for RS-232 for the serial interface SERIAL0 of the SAB80C537.

A44 R10 Receiver 1 Output

Output:Already connected with RxD0 of the controller. For other utilization, cut the connection with RxD0.

Free RS-232-Driver connections

The following connections of the RS-232-driver chip are at one's disposal. They can be used for the second serial interface SERIAL1 or for handshake-signals.

A49	R3I	(RS-232)	A50	R30	(TTL)
A55	R2I	(RS-232)	A54	R20	(TTL)
A45	R1I	(RS-232)	A44	R10	(TTL)
A56	T40	(RS-232)	A52	T4I	(TTL)
A48	T30	(RS-232)	A51	T3I	(TTL)
A46	T20	(RS-232)	A43	T2I	(TTL)

RS-485-Driver connections

B29 RS-485_VCC

Voltage supply for the RS-485-Driver chip. Can be switched on/off externally if the connection is cut.

B31 RS-485-signal B
B33 RS-485-signal A

Inputs/Outputs that are the complementary data-signals to RS-485. For connections with up to 31 other modules, don't exchange A and B.

B30 D Transmit-data-input (TTL)

Already connected with TxD 1 at B57 (port 6.2)
For the utilization for other purposes of this driver please cut the connection B30-B57.

B32 R Receive-data-output (TTL)

Already connected with RxD 1 to B56 (port 6.1)
For other applications of this driver please cut the connection B32-B56.

B34 /R Inverse receive-data-output (TTL)

Already connected with A17 (port 3.2, /INT 0) for PHYNET.
For other applications of P3.2 open JP6.

B36 /RE RS-485-Receiver_Enable

Input: Already connected with B52 (port 5.0) for PHYNET.
For other applications of P5.0 cut connection B36-B52.

B35 /DE RS-485 Transmit-Enable

Input: Already connected with B51 (port 5.1) for PHYNET.
For other applications of P5.1 cut connection B35-B51

General Control signals

A57 ALE	Address-Latch_Enable, see controller manual
A31/ PSEN	Program_Store_Enable,see controller manual
A22/ RD (Port 3.7)	see controller manual
A22/ WR (Port 3.6)	see controller manual
A36/ WRO	Write_Out (Write-pulse unbuffered, can be turned-off)

Output active LOW. This signal corresponds to the /WR-signal, but can be disabled by a RESET or the M-DIS-function. For missing supply voltage this signal has no voltage.

A37/ PWR Protected_Write (Write-pulse buffered, can be turned off)

Output active LOW. This signal corresponds to the /WR-signal, but can be disabled by a RESET of the M-DIS-function. For missing supply voltage, this signal has battery voltage and can therefore be used for external components with battery buffering.

A61 /RESIN RESET-Input

Input active LOW. A connection with GND for about .5 sec. triggers a RESET-pulse. Permanent connection causes a cyclic RESET-pulse series of 1.6 sec duration. This input is not appropriate to stop the controller for the duration of the activation of /RESIN.

A34 /RES RESET-Input/Output

Input/Output active LOW. This bi-directional connection might be connected to GND. For the duration of this connection the controller remains in the status of a continued RESET. The actuation of the /RES should be bounce free. The slope of rising edge depends on the load capacity.

A33 RES RESET-pulse output

Output active HIGH. This signal provides the inverse RESET-pulse of /RES.

Attention:
An external RESET by wiring of A35 (/RES) doesn't generate a signal at A33. Only the RESET-pulses triggered by A61 will be present.

A13 BRESBattery-supplied RESET-signal

Output active HIGH. This signal is the inverse of /RES.

If battery-back up is available, the signal is connected to the battery voltage during missing supply voltage VCC.

This output should not be loaded to much and can cause a quick discharge of the battery in case of unfavorable external circuits.

A14 RES 2 RESET-signal without battery back-up

Output active HIGH. This signal is the inverse of /RES, as long as VCC is within the tolerated voltage range. If the supply voltage VCC is failing, this connection doesn't provide a valid signal. A discharge of the external battery is not possible.

A40 LOWLIN Voltage-Failure Signal

Output: This signal is HIGH, as soon as the supply voltage drops below the limit of 4.6 or 4.8 V. It is LOW, as soon as the supply voltage is above this limit. This output should not be loaded very much, since the battery buffering might be disturbed.

A12 /OFF Memory-De-selection-Signal

Output active LOW. This signal gives rise to the de-selection of the volatile memory and disables a write signal during turn-on procedure of the supply voltage VCC. This signal can be used for external components, but should not be loaded extensively.

A11 M-DIS Memory-Disable

Input active HIGH. This signal can be used for the de-selection of the volatile memory. (Power-Down). As long as this input is LOW, only the failure of the supply voltage will cause a de-selection. If this input is wired, the connection at JP5 has to be removed.

A53 RS-DIS RS-232-Disable

Input active LOW. This signal is used to turn-off the RS-232 driver chip and can also be applied for sensitive applications to reduce the current.

B27 B0 Bank-Select 0
B28 B1 Bank-Select 1

Inputs: If a 128 kByte-RAM is installed in U13 the highest address bits are provided and can be connected with the appropriate port connections.

A39 PFI Power-Fail-Input
A38 /PFO Power-Fail-Output

Input: This signal can be used to recognize beginning power failures of the power supply. The output /PFO can be utilized to create an interrupt.

A69 /WDP Watchdog-Pulse
A35 /WDO Watchdog-Output

/WDP is an input. Cyclic signal alterations within one second at /WDP don't trigger a RESET. The failing of these pulses entails a RESET and a signal at output /WDO. /WDP should be open if not used.

B54 /PE Power-Down_Enable, Start_Watchdog

The input is already connected with GND and influences the controller-internal watchdog-timer and blocks the power-down-mode. Please read the controller manual from INFINEON for more information. If this input should be connected externally, cut the connection at J4.

The listing of the module-terminals already connected

In order to operate the miniMODUL-537 with a minimum of external connections, the serial interfaces of the controller are already connected with the driver-chips. The conducting-stripes are close to the edge of the circuit board and are easily cut.

Terminals of the RS-485-interface already connected:

B29	VCC485	with B01	(VCC)
B30	(D)	with B57	(TxD1, Port 6.2)
B32	(R)	with B52	(RxD1, Port 6.1)
B34	(/R)	with A17	(INT0, Port 3.2) with jumper JP6
B35	(DE)	with B51	(Port 5.1)
B36	(/RE)	with B52	(Port 5.0)

Terminals of the RS-232-interface already connected:

A44	(R10)	with A15	(Port 3.0, RxD)
A41	(T1I)	with A16	(Port 3.1, TxD)

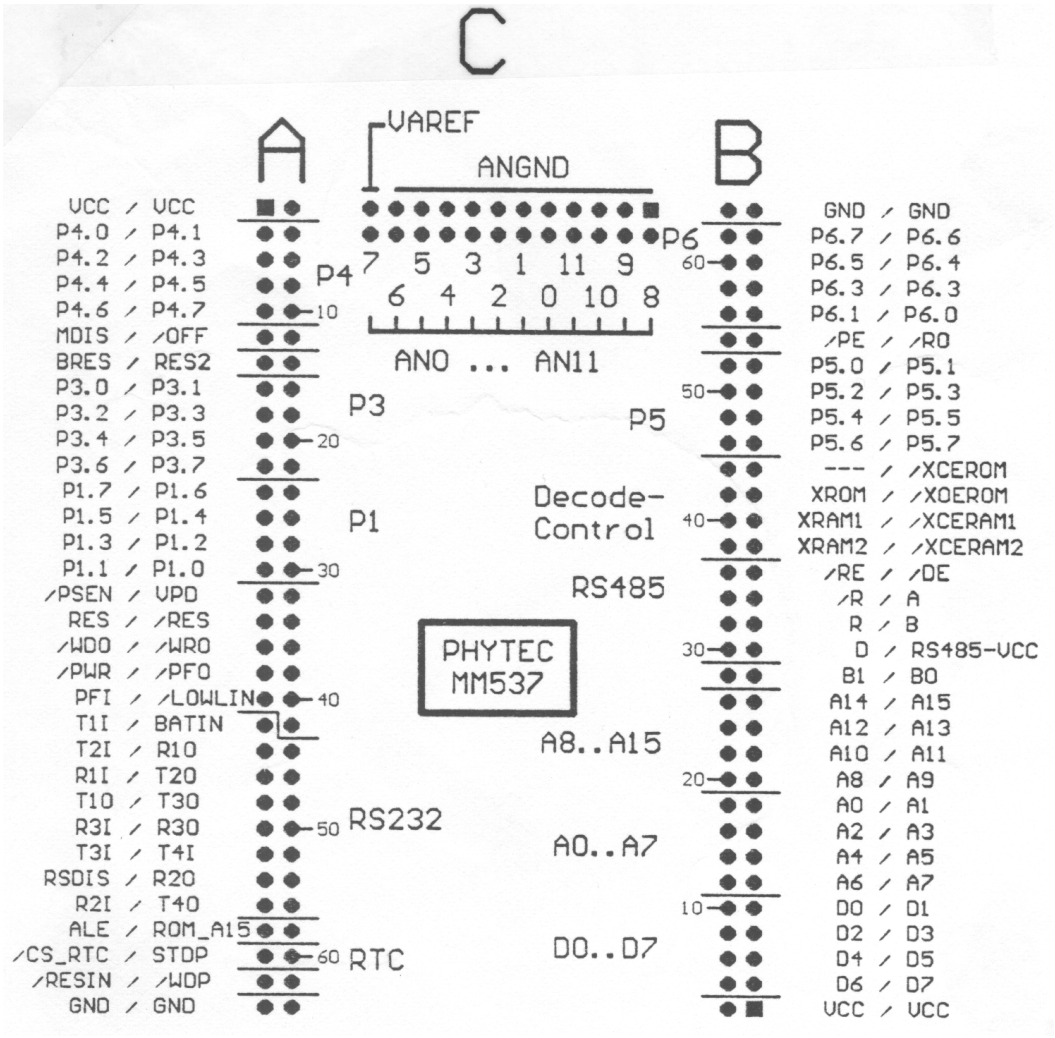

Figure 3: The terminals of the miniMODUL-537

4 Memory Configuration and Address-Decoding

4.1 Standard-Memory-Configuration

The miniMODUL-537 allows different memory configurations, which depend on the memory chips and on some jumper settings. In general the memory chips are selected in blocks of 32 kByte. Chip-enable signals with a finer partitioning is not possible with the decoder of the module. This can be achieved with an external chip.

Despite of the simple, module-internal address-decoding, the miniMODUL-537 doesn't restrict the address decoding for special applications. By the possibility to turn off the module-internal decoding externally, you are absolutely free for your own address decoding. On request we program PALs, GALs and EPLDs according to customer specifications.

The standard installation is 32Kbyte RAMs and 0 or 32 kByte EPROMs. The maximum EPROM capacity is 64 kByte. The maximum RAM capacity is a 128K*8 SRAM in U13. (Available according to the manufacturer in the middle of 1991). U13 is prepared for this RAM chip. The RAM is accessed in one of the four 32 kByte memory banks. The bank-selection is achieved by the two external connections B0 and B1, which can be connected to arbitrary port pins. With the maximum capacity in U12 a total maximum of 160 kByte RAM can be installed.

Optional in U12 also a 8/32 kByte EEPROM can be installed.

4.2 Von-Neumann-Memory-Configuration

The data-memory in U12 and U13 is independent from the program-memory U11, since the controller selects separately both memory types with the control signals /PSEN and /RD, /WR. For special applications the RAMs U12 and U13 can be selected as data- or program-memory (Von Neumann-Model). The program-memory selected in the RAM must be subtracted from the capacity available in the EPROM. The configuration of both RAMs as data- or program-memory is selected by jumper JP11. The connection of the /RD-terminal of the RAM with the signal /VN results in the combined data- program-memory. The connection with /RD allows only data-memory access to the corresponding RAM. The following section describes the jumper-configurations in more detail.

4.3 The Individual Memory-Configurations

The miniMODUL-537 has only the address-decoder A15. Nevertheless other memory-configurations are possible. For this purpose few external components or a special PAL/PLD have to be connected, which can be delivered by us. The miniMODUL-537 has separate control inputs, which can be used to turn off the address decoder of the module. Then external CE-signal determine the memory configuration. Besides the access-mode and the addressing range also other adjustments have to be made, which depend on the utilization of the components.

4.4 External Extensions with more Memory-Chips

An additional possibility has also to be mentioned: by external wiring more memory chips or other peripherals can be connected to the data/address bus. The required control signals are easily externally produced by standard components or an external PLD. Since all bus and control signals are externally completely available, the connection of an external EPROM in DIL-housing, a DUAL-Port RAM or other peripherals is very easy accomplished.

4.4.1 Application of an External DIL-EPROM

If the application of an EPROM with LCC-housing is not possible, a standard EPROM with DIL-housing and up to a capacity of 64 kByte can be connected externally. In this case no EPROM is installed in U11. All control and bus signals of the LCC-EPROM-socket of the module are conducted outside. As control-line use B41 (/XOEROM) and (/XCEROM) or externally produced control signals.

4.4.2 Application of an EEPROM

Independently if an EEPROM is used in U12 or an external EPROM is employed, the following hints should be observed:

Use only VCC for the supply voltage. Don't forget to adjust U12 with jumper JP12 to VCC (battery might be discharged.)

Pay attention for 8 kByte-EEPROMs to pin 1. For some chips this is a Ready/Busy-Output, which disturbs the function of A14. In this case pin 1 should not be connected with A14. Also consider, that JP14 has to be open.

Some EEPROM chips consume considerable current at the /WR-input, pin 27. This causes a quick discharge of the battery for the RAM and Real-Time Clock. Therefore don't use the write-signal /PWR for EEPROMs. Also the controller signal /WR is not appropriate, since for this controller-family the write-signal is on GND until the transient recovery voltage of the system-clock is stable. Otherwise overwriting during the turn on procedure would be caused. Please use the write-signal /WRO. U12 can be adjusted with JP15 to this mode.

4.5 Address Decoding

The memory chips are selected by address-bit A15. The access-mode to the EAM (data- program-memory or mere data-memory) is chosen by the jumpers JP11a and JP11b. The address range of the RAM is selected by jumper JP7a and JP7b.

The address decoding is determined by the jumpers JP7,JP11 and JP8. U10 allows the turning off of the module-internal decoding and JP9 the 'Power-On-Jump' to the address 8000H.

The externally controlled signal-drivers of U10, which can be turned off, can drive separately U11,U12 and U13. The signal XROM disables the selection of the module of CS_ROM and OE_ROM. XRAM1 influences the selection of RAM1 in U13 and XRAM2 the selection in RAM2 in U12.

In the case that the signals XROM, XRAM1 and XRAM2 are open or HIGH, the module-internal decoder is active. As soon as those signals are LOW, the corresponding inputs are floating, which allows the utilization of an external decoder.

4.6 Hints for Memory Utilization

The SAB80C537 separates data- and program-memory. By appropriate address decoding both memory types can be combined in one physical memory chip. The miniMODUL-537 is very flexible for the memory-configurations, memory-types and their application.

For save operation we want to give the following recommendations.

Operable machine-programs should be stored in their final version in the EPROM. Despite battery back-up a bit could be missing by external influence with the result, that the program doesn't operate anymore, which even the watchdog-timer can not prevent. The storage in the EPROM is always the safest method.

For the storage in RAM or EEPROM, of remote transmitted programs to the miniMODUL-537, a program-kernel and an error-recognition and error-treatment concept should be available in the EPROM.

As long as the access-time to the EEPROM is not less than 200 ns, the machine-program should not be operated from the EEPROM. The duration of one command-cycle of the SAB80C537 is about 215 ns for 12 MHz.

4.7 The Power-On-Jump-Option

This option allows the storing of the program during testing in the address region of the RAM, where finally the EPROM is installed. This makes easy the handling of interrupt-vectors, which are stored in the program-memory in the region 100H. This feature is used by our combined Monitor-Basic. It is advisable not to start those programs at 0000H, but at 8000H. Nevertheless to allow a program-start after a RESET, special precautions have to be taken for hard- and software.

The hardware-RESET resets the Power-On-Flipflop U9. This selects the EPROM in the region starting at 0000H and its content is reflected from 8000H to 0000H. Other memory-chips are disabled for this operation. The first machine cycle must be a LJMP 8xxxH. With this command the jump is realized.
With the first command-cycle to an address higher or equal to 8000H the Power-On-Flipflop is set. Therefore the EPROM is selected only as program-memory for addresses higher than 8000H. Below 8000H the RAM is free available.

Please consider the special note for the installation in *section 5 'Jumper Description'* concerning D8. For layout versions later 1021.2 this note is obsolete.

4.7.1 The Realization of User Programs in Power-On-Jump-Mode

User programs can be stored for test-purposes with Monitor-Basic starting at 0000H. Only for transition to an EPROM the following has to be observed:

The program must be linked to addresses higher/equal 8000H. The first machine command of the program at the address 8000H is LJMP 8xxxH. 8xxxH is the cold-start point of the user program.

Programming of the maximum 32 kByte EPROM starts at the physical address 0000H. This address is at 8000H during the program operation and in the memory region of the controller. For this reason a special address-setting command of the EPROM-programmer has to be used, otherwise the programmer tries to program to the address8000H which doesn't exist or gives an error message.

4.7.2 Program Example

```
ORG 8000H              ;(or absolute in the Link-Batchfile)
LJMP START     ***     ; position for vectors, tables etc. ***

ORG 8xxxH              ;(or stated in the Link-Batchfile)

START                  ; Start of the program
```


5 Jumper Description

In order to be flexible with the miniMODUL-537 a series of jumpers are installed. Those determine the application of various memory chips, the memory-configuration, some controller adjustments, interface connections and control functions for the Power-Down-operation. In the following the jumpers and their functions are listed:

JP1	Influences the time-constant of the monitor-chip
JP2	Selection of the controller external program-memory U11
JP3	Oscillator-Watchdog-Enable (See controller manual SAB80C537)
JP4	PD-Enable, Watchdog-Inhibit
JP5	Memory-Disable. Already connected to GND
JP6	RS-485-Interrupt
JP7	RAM-address-selection
JP8	ROM-address-selection
JP11	For the selection of the RAM-memory type U12/U13
JP14	For switching-off of the RS-232-driver. Already connected to operation
JP9,JP10	EPROM-type selection. Already connected for 32 kByte-type EPROM.
JP12,JP13,JP15	RAM/EEPROM-selection for U12

The jumper JP2, JP3, JP4, JP5, JP9, JP10, JP13 and JP14 are already connected. For modifications please cut the connections of the copper conducting stripes.

5.1 Jumper for Address Selection

The following statements for the memory-configurations refer only to the module-internal address-decoding. They don't represent a restriction for the application of the module. You are always able to choose any memory-configuration for your application, by the utilization of external address decoders.

JP7a and JP7b RAM-address selection for U12 and U13

For jumper 7 A15 or /A15 is selected as /CE-signal for RAM U12 and U13. Those jumpers are positioned before driver U10, which can be switched off, so that their position is ineffective for the external de-selection by XRAM1 and XRAM2.

The connection with A15 selects the range 0000H..7FFFH.
The connection with /A15 selects the range 8000H..FFFFH.

For the configuration of the jumpers use the jumper-diagram.

JP11a and JP11b program/data memory selection for U12 and U13

With jumper 11, /RD or /VN is used to connect the data with the databus. In the position to /RD only data-memory access is possible. For the position to /VN the corresponding RAM is selected as program-memory. It is obvious, that the address region of the region selected as program-memory can not be selected for the EPROM.

JP12, JP13 and JP15 RAM/EEPROM-selection for U12

In U12 a RAM or EEPROM with a maximum of 32 kByte can be installed. Corresponding is the configuration of the three jumpers. Please use the following table:

Installed	RAM	EEPROM
JP12	Connection with VCC or VPD	
		Connection with VCC
JP13	Connection	Don't connect for 8K-EEPROM
JP15	Connection with /PWR	
		Connection with /WRO

Please pay attention to the jumper diagram.

JP8 EPROM-address selection for U11

Jumper JP8 allows different addressing modi for the EPROM U11. The middle pads are connected. They should never be separated.

Connection of the middle pad of JP8 with GND

The EPROM U11 is always selected as program-memory. Data-access to U11 is not possible. To read text files use the machine-command MOVC.
The RAM/EEPROM can be selected only as mere data-memory.

The connection of the middle pad of JP8 to A15

The EPROM U11 is selected only in the addressing range 0000H..7FFFH as mere program-memory. Data-memory access to the EPROM is not possible. To read text files from the EPROM use the machine command MOVC. The RAM/EEPROM can be selected in this range only as mere data-memory. In the range 0000H..7FFFH the RAM can be selected as combined program/data-memory.

Connection of the middle pad of JP8 with POJ

With this configuration the Power-On-Jump option is selected. After the program start, the EPROM U11 is selected only in the range 8000H..FFFFH. However after a RESET automatically a jump is executed to this region. For address 0000H no machine-program is necessary, since the EPROM is reflected temporarily to 0000H. Please pay attention to the hints in the separate section of this topic.

Important Note (only for layout-version 1021.2):

Selecting the POJ-mode, a change of the installation of diode D8 is required. D8 is found adjacent to JP7, above the printing of JP2. The cathode (blue ring) is at the side of the neighboring diode.

Please install this diode, in case that you use the POJ-mode.
Please remove this diode, if you select a different mode.

We reserve us the right to solder this diode on one or both ends to the circuit board corresponding to the order. A later redesign of the circuit board layout will add an additional jumper for this purpose.

If you will have no RAM-access, despite proper program start at 8000H, you might have forgotten to remove the diode D8.

JP9 and JP10 EPROM-Type selection

JP9 and JP10 determine the type of the EPROM installed in U11. This jumper is found at the component side of the circuit board and is already connected for a 32 kByte EPROM. For an externally connected EPROM this setting is meaningless.

Those jumper select the signals A14,A15 and VPP for 8, 16, and 32 kByte EPROM. Please use the jumper diagram, where all possible configurations are indicated.

5.2 Jumper for Controller Pre-Configuration

JP2, JP3 and JP4 Controller pre-configuration

With these jumpers controller-internal pre-configurations are made, which are described in the controller manual.

JP2 /EA selection internal/external program

Already connected with GND. As long as this jumper is connected with GND, program-memory access is executed also below 2000H of the program-memory U11. A change is necessary only for mask-programmable controllers.

JP3 Oscillator-Watchdog-Enable

Already connected with GND. Please pay attention to the description found in the controller manual.

JP4 /PE-SWD Power-Down and Watchdog-Enable

Already connected with GND. Please pay attention to the detailed description in the controller manual.

5.3 Jumper for Power-Down-Operation

JP5 Memory-OFF

Already connected to GND. For applications which temporarily require low power-consumptions, the memory of the miniMODUL-537 can be deselected by external wiring of the M-DIS connection. If this is not required, jumper JP5 remains in its position, otherwise the connections have to be removed carefully.

JP14 RS-232-Disable

Already connected to GND. For applications, which temporarily require low power-consumption, the interface driver U4 of the mini-MODUL-537 can be deselected by external wiring of the connection RS-DIS. If this is not required, jumper JP14 remains in its position, otherwise the connection has to removed carefully.

5.4 Jumper for Connection of the Interface Driver

The standard interfaces SERIAL0 and SERIAL1 are already connected with easy to cut conduction stripes adjacent to the edge of the circuit board. Only for the operation of the RS-485 interface with the software of PHYNET the jumper JP6 at the top of the circuit board has to be closed.

JP6 RS-485-interrupt for PHYNET

For the standard-configuration open. Is only used for the operation with PHYNET.

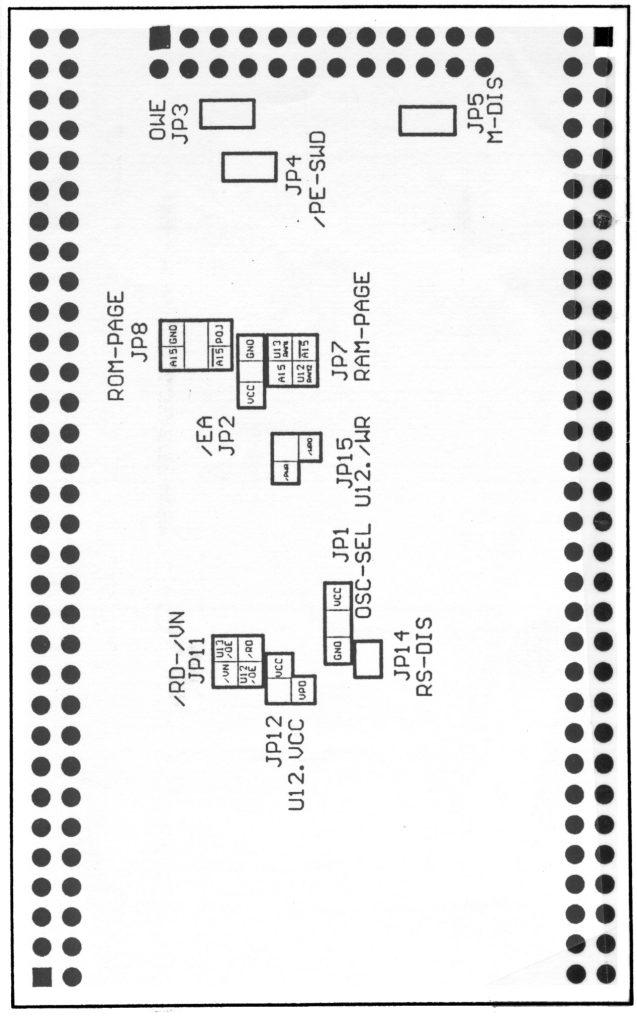

Figure 4: Jumper

6 The Serial Interfaces

One of the most used components of the controller-peripherals are the serial interfaces which are described in the following. Even so the SAB8053x controllers are compatible to the higher version of the 8031-family, there is one difference in the generation of the baud rate. For the attempt to employ 8031-software, this should be recognized.
The controller SAB80C537 has two asynchronous, serial interfaces SERIAL0 and SERIAL1, which can be programmed separately and operated with different baud rates at the same time. Both interfaces can transmit and receive simultaneously. The interfaces can be polled by software or operated with interrupts.
The function of the interfaces is adjusted with a set of special-function-registers (SFR), which are mentioned short at this point. The detailed description is found in the controller manual *section 7.2* beginning at page 72.

6.1 The Special-Function-Register of SERIAL0

S0CON Controller register
Serves for mode-selection, for the determination of the transmission format and contains the important status bits RI0 (RI) and TI0 (TI)

S0BUF Data-buffer register
Stores the data-byte to be received or transmitted. In reality one transmission and one reception buffer exists.

BD Bit for the baud rate generator selection
This bit is found as an exception in the SFR AD-CON of the analog-digital converter. The bits can be addressed. To generate the baud rate the fixed baud rate generator or timer 1 can be used.

SMOD Bit for the determination of the division ratio of the baud rate. Setting this bit, doubles the baud rate. It is found in the register PCON and is not bit addressable.

6.2 The Baud Generator of SERIAL0

For the serial interface SERIAL0 the internal baud generator can be selected by setting bit BD. This requires a system-clock cycle of 12 MHz. The baud rates 4800 and 9600 are possible depending on the bit SMOD.

For other baud rates timer 1 has to be used as baud generator. Then this timer can not be used anymore during the data transmission for other purposes.

Timer 1 is used as baud generator, as long as bit BD is not set. For this version timer 1 must be also initialized and started. For these purposes the registers TMOD, TCON and TH1 are available. As an example we refer to the following assembler program. To generate proper baud rates the system-clock frequency must be appropriate. The standard frequency of timer 1 is 11.059 MHz.

For deviating frequencies calculations have to be done according to the computation rules in the controller manual, if the required baud rates can be generated with the gradation which is necessary for the reload-register TH1. In the following you find a table with all possible baud rates for the standard frequency of 12 and 11.059 MHz.

The controller versions with 16 MHz can be operated for SERIAL1 at 9600 and 4800 baud. For SERIAL0 no sufficient accurate adjustment for this baud rate at 16 MHz is possible.

Table of the baud rate for the frequencies 12 and 11.059 MHz.

Baud rates for f=12 MHz			**Baud rates for f=11.059 MHz**		
TH1	**SMOD=0**	**SMOD=1**	**TH1**	**SMOD=0**	**SMOD=1**
255	31250.00	62500.00	255	28799.48	57598.96
254	15625.00	31250.00	254	14399.74	28799.48
253	10416.67	20833.33	253	9599.83	19199.65
252	7812.50	15625.00	252	7199.87	14399.74
251	6250.00	12500.00	251	5759.90	11519.79
250	5208.33	10416.67	250	4799.91	9599.83
249	4464.29	8928.57	249	4114.21	8228.42
248	3906.25	7812.50	248	3599.93	7199.87
247	3472.22	6944.44	247	3199.94	6399.88
246	3125.00	6250.00	246	2879.95	5759.90
245	2840.91	5681.82	245	2618.13	5236.27
244	2604.17	5208.33	244	2399.96	4799.91
243	2403.85	4807.69	243	2215.43	4430.69
242	2232.14	4464.29	242	2057.11	4114.21
241	2083.33	4166.67	241	1919.97	3839.93
240	1953.13	3906.25	240	1799.97	3599.93
239	1838.24	3676.47	239	1694.09	3388.17
238	1736.11	3472.22	238	1599.97	3199.94
237	1644.74	3289.47	237	1515.76	3031.52
236	1562.50	3125.00	236	1439.97	2879.95
235	1488.10	2976.19	235	1371.14	2742.81
234	1420.45	2840.91	234	1309.07	2618.13
233	1358.70	2717.39	233	1252.15	2504.30
232	1302.08	2604.17	232	1199.98	2399.96
231	1250.00	2500.00	231	1151.98	2303.96
230	1201.92	2403.85	230	1107.67	2215.34
229	1157.41	2314.81	229	1066.65	2133.29
228	1116.07	2232.14	228	1028.55	2057.11
227	1077.59	2155.17	227	993.09	1986.17
226	1041.67	2083.33	226	959.98	1919.97
225	1008.06	2016.13	225	929.02	1858.03
224	976.56	1953.13	224	899.98	1799.97
223	946.97	1893.94	223	872.71	1745.42
222	919.12	1838.24	222	847.04	1694.09
221	892.86	1785.71	221	822.84	1645.68
220	868.06	1736.11	220	799.99	1599.97
219	844.59	1689.19	219	778.36	1556.73
218	822.37	1644.74	218	757.88	1515.76
217	801.28	1602.56	217	738.45	1476.90

216	781.25	1562.50	216	719.99	1439.97
215	762.20	1524.39	215	702.43	1404.85
214	744.05	1488.10	214	685.70	1371.40
213	726.74	1453.49	213	669.76	1339.51
212	710.23	1420.45	212	654.53	1309.07
211	694.44	1388.89	211	639.99	1279.98
210	679.35	1358.70	210	626.08	1252.15
209	664.89	1329.79	209	612.75	1225.51
208	651.04	1302.08	208	599.99	1199.98
207	637.76	1275.51	207	587.74	1175.49
206	625.00	1250.00	206	575.99	1151.98
205	612.75	1225.49	205	564.70	1129.39
204	600.96	1201.92	204	553.84	1107.67
203	589.62	1179.25	203	543.39	1086.77
202	578.70	1157.41	202	533.32	1066.66
201	568.18	1136.36	201	523.63	1047.25
200	558.04	1116.07	200	514.28	1028.55

6.3 The Special-Function-Register of SERIAL1

S1CON Control Register
Serves for the mode selection, for the determination of the transmission format and contains the important status bits RI1 and TI1.

S1BUF Data-buffer register
Stores the data-byte to be received and transmitted. In reality a transmission and reception buffer exists.

S1REL baud rate register
The content of those registers determine the baud rate of SERIAL1. For 12MHz system-clock frequency a range of 1.5 KBaud to 375 KBaud can be covered.

6.4 The Baudrate-Generator of SERIAL1

The separate baud rate generator of SERIAL1 can be set to the required baud rate by the register S1REL. For 12 MHz system-clock frequency the region is positioned in a way, that all standard baud rates can be configured. Antiquated low baud rates can not be realized with 12 MHz. The region of adjustable baud rates is within the range of 1.5 KBaud to 375 KBaud. The exact computational rules are found on page 82 in the controller manual. For deviating frequencies calculations have to be done according the computation rules in the controller manual, if the required baud rates can be generated with the gradation, which is necessary for the baud rate register S1REL.

The controller versions with 16MHz system-clock frequency can be operated for SERIAL1 at 9600 and 4800 baud. For SERIAL0 no sufficient accurate adjustment for the baud rate at 16 MHz is possible.

6.5 The Connection to the Interface Driver

The miniMODUL-537 has four transmission and three reception channels with RS-232 standard and can be wired arbitrarily. The driver can be used for SERIAL0, SERIAL1 or for control lines of handshake hardware.

Corresponding to the most frequently used applications, some of the drivers are already connected with the interface of the controller. This has to be considered for user interface configurations. The connections are placed close to the edge of the circuit board and are easily separated.

6.5.1 Connections of the RS-485-Interface Pre-Configured

The connections of the serial interface SERIAL1 are prepared for the utilization as RS-485-interface. This bi-directional interface requires besides the two symmetric data-lines, control signals, which are already connected for the miniMODUL-537 with certain controller port pins. In addition to the controller connections TxD1 (P6.2) and RxD1 (P6.1) also port bits P5.1 and P5.0 are connected. For other utilization of the port bits the connections at the edge of the circuit board have to be separated. The link with P3.2 (/INT0) is achieved via the jumper JP6.

B29	VCC485	with B01	(VCC)
B30	(D)	with B57	(TxD1, Port 6.2)
B32	(R)	with B52	(RxD1, Port 6.1)
B34	(/R)	with A17	(INT0, Port 3.2) by jumper JP6
B35	(DE)	with B51	(Port 5.1)
B36	(/RE)	with B52	(Port 5.0)

6.5.2 Connections of the RS-232-Interface Pre-Configured

The interface SERIAL0 is prepared as interface of the RS-232 standard with the corresponding connections. For this purpose the transmission and reception driver R1 and T1 of the driver chip U4 are used for RxD0 and TxD0.

The other driver and reception connections are vacant, since the standard software from PHYTEC doesn't use hardware handshaking.

A44	(R10)	with A15	(Port 3.0, RxD)
A41	(T1I)	with A16	(Port 3.1, TxD)

6.5.3 The Pin Assignment of the Interface for the miniMODUL-537

For better recognition of the interface connections with RS-232 standard the data-in/outputs are emphasized at the print of the circuit board. The arrows indicate the direction of data-flow. The connections of the RS-485 interface are also emphasized at the print of the circuit board.

6.6 General Remarks for RS-232 and RS-485 Interfaces

6.6.1 RS-232 Interface

The serial data transfer with RS-232 standard is only appropriate for the connection of two participants via relative short distances of a about 10m. The baud rate, that can be employed depends very much on the length and type of the connection cable. Standard baud rates for the communication are 9600 and 19200 baud for interoffice applications. The transmission of data in one direction require one line (RxD, TxD). In addition to GND also control lines might be used, which influence the flow of data. All PHYTEC-controller boards use RS-232 interfaces without control lines. The mutual overflow control is achieved by software-handshaking. For the XON-XOFF protocol the reserved signs 11H and 13H are added in the data-flow for control purposes. This requires, that the handling of the protocol of the participants is adapted to each other. Otherwise transmission errors, loss of characters or locking might occur. Therefore we recommend the application of our communication software. Because of this protocol, only ASCII-coded signs and a restricted number of character sets can be transmitted.

6.6.2 RS-485-Interface

The transmission with RS-485 standard allows a maximum of 32 participants for a two wire line. In comparison to the RS-232 interface higher baud rates and line length are possible. The maximum transmission rate of the SAB80C537 with 1 Mbit/sec for a system-clock frequency of 12 MHz can be achieved. Since 32 participants can be connected to the two wire line for this standard more control and protocol management is required than for the RS-232 interface. The transmission with RS-485 standard operates with a two wire bi-directional line with alternating directions. Both ends of the line are terminated with resistors. The symmetric data-transfer of the two wire line considerably improves the immunity against interfering.

The cross linkage of these modules in the industrial environment requires specific knowledge of the occurrence of the special problems. Interferences from electromagnetic devices in the surrounding, potential differences of different stations and the effect of ground loops have to be considered. For such purposes the galvanic separation of processor and network are advisable.

6.7 Changing from RS-232 to RS-485 Standard

The RS-232 interface cannot be modified to RS-485 without additional software. For such a project it is also important to know if the participants are operating in a master-slave or multi-master network. In addition to the data-inputs also the inputs of the driver chips of all stations have to be controlled in a skillful way. Therefore PHYTEC has developed a software with the designation PHYNET for the communication with RS-485 interfaces. With this software all modules with RS-485 interface can be interconnected with a network.

6.8 Program Example for the Serial Interface

The given examples use no interface interrupts, but test only the interface flags RI and TI.

6.8.1 Program for SERIAL0

```
; Example of the initialization for the utilization of the
; internal baud rate generator for 12 MHz system-clock frequency.

init: setb  BD    ; Select internal BD-generator
      orl   PCON,#80H   ; Set bit SMOD for 9600 baud
                  ; Alternative: anl PCON,#7FH for 4800
            ; baud
      mov S0CON,#5AH    ; Mode-adjustment and initialization
                  ; of the flags RI0 and TI0 8
                  ; data bit, no parity, 1 start bit,
                  ; 1 stop bit TI0 set, RI0 erased.
init_end:   ...
      ...

; Example of the initialization for the utilization of timer 1
; as baud rate generator for a system-clock frequency
; of 11.059 MHz.

ch0_in:                 ; Subroutine to read a character
      jnb RI0,ch_in     ; Wait until character accepted
      clr RI0
      mov a,S0BUF
      ret         ; character in ACC

ch0_out:                ; Subroutine to output a character
                  ; Output character in ACC
      jnb TI0,ch_out    ; Wait until ready for transmission
      clr TI0,ch_out
      mov S0BUF,a
      ret

init: clr BD      ; not necessary after a RESET
      anl TMOD,#0FH
      orl TMOD,#20H     ; Mode 8 bit, autoreload
      orl PCON,#80H     ; Set bit SMOD Baud
                  ; Alternative: anl PCON,#7FH
      mov TH1,#232      ; Reload value for 2400 baud for SMOD=1
      setb TR1    ; Start timer 1
      movb S0CON,#5AH   ; Mode adjustment and initialization of
                  ; flags RI0 and TI0 8 data bit, no
                  ; parity, 1 start bit, 1 stop bit set
                  ; TI0, Erase RI0
init_end:   ...
```

6.8.2 Program for SERIAL1

```
; Example of initialization of SERIAL1 for 19200 baud
; for 11.059 MHz system-clock frequency.

init: mov   S1REL,#238  ; Reload value for 19200 baud
      mov   S1CON,#92H  ; Mode-adjustment and  initialization
                  ; of the flag RI1 ; and TI1, 8 data
              bit,
                  ; no parity 1 start bit, 1 stop bit
                  ; Set TI1, erase RI1
init_end:   ...
      ...


ch1_in:     ; Subroutine for reading a character from SERIAL1

      mov   a,S1CON
      jnb   ACC.0,ch_in ; Wait until character received
      anl   S1CON,#0FEH ; Reset RI1
      mov   a,S1BUF
      ret         ; character in ACC

ch1_out:    ; Subroutine for outputting a character
      ; Output character in ACC

      push  ACC
w_out:      mov   a,S1CON
      jnb   ACC.1,w_out ; wait until TI1 ready for transmission
      anl   S1CON,#0FDH ; Reset TI1
      pop   ACC
      mov   S1BUF,a
      ret
```


7 RAM-Write-Protection and Battery Back-up

Write-protection and battery back-up are achieved by U3, U6, and Q2..Q4. An external battery must be connected to A42. The current consumption from VPD depends on the type of RAM and their extensions. Installing a good 32 kByte RAM (1µA) a 100 mAh battery will do for several years.

The RAMs U12 and U13 and the optional Real-Time Clock U14 (RTC 72421) are supplied by the battery as soon as VCC decreases below 4.6 or 4.8 V. U12 is either supplied with VCC or VPD. This is adjusted by jumper JP12. If an EEPROM is installed, jumper JP12 must be adjusted to VCC. A RAM in U12 can be supplied by VCC or VPD.

If you forget to set jumper JP12 correctly, the battery will be discharged quickly if an EEPROM is installed in U12.

7.1 Function of the Battery Buffering and Write Protection

The RAM chip and the RTC are deselected with the signal /RES. U3 is a µP-monitor chip, which detects the short fall below 4.6 or 4.8 V of the supply voltage, and switches immediately the signal /RES to LOW. U6 transmits this signal to the transistors Q2..Q4, which deselect the RAMs and cut off currents from the battery to the driver outputs of U10. In the battery back-up operation U3 supplies the RAMs and the RTC with the battery voltage VPD. The maximum permissible current from U3.2 (VOUT) is 50mA. If this value is exceeded, or the voltage drop is too high, Q1 should be installed. This results in a considerable increase of current consumption from the battery. Then a capacity of 100mAh might not be sufficient anymore. U3 serves for the purpose to decouple the /RES signal and improve the pulse shape. To avoid the malfunctioning of the write-protection, the /RES signal should not be loaded too much. /RES remains after turn on of the supply voltage for about 50msec low active. Hereby disturbing write pulses of the processor before the start of the system clock are suppressed. For turn off U3 separates the /WR signal from the memory chips and the RTC.

It should be recognized, that the functioning of the write-protection only works, if the supply voltage is applied and separated bounce free.

7.2 Hints for the Utilization of the Battery Buffering

The safety of a circuit with battery buffering for volatile memories with write-protection is generally overestimated. A battery buffered RAM never replaces an EPROM. It is not advisable to use a battery buffered RAM for long term storage of programs. Already a program crash stimulated externally, might overwrite critical partitions of the RAM. The battery buffered RAM should be used only for data and parameter storage.

A most reliable circuit for write-protection during the application and removing of the supply voltage, must include the power supply and the voltage regulator, which is not incorporated in this case.

The RAM should be used as program memory only if the program can be down loaded easily or if the program is redundant and can be loaded from an EPROM.

You minimize problems with the RAM write-protection, if you observe the followings advices:

Provide a well defined, bounce-free decrease and increase of the supply voltage VCC. The unplugging of the module in the operational status and the turn on/off procedure of the regulated voltage VCC with mechanical contacts might overcharge the write-protection.

Wire the supply voltage before the voltage regulator and provide sufficient capacitors to achieve a defined voltage transition.

Provide, if required, checksum or other redundancy to recognize memory errors and means to correct them, independently if you use the RAM as data- or program- memory.
The application as program-memory makes only sense, if the programs can be reloaded easily. In case of doubt, use an EPROM as program-memory.

The probability of a memory-error is negligible, but cannot be excluded. Please consider this fact for your application.

8 The External Watchdog-Timer and the Power-Fail-Option

The monitor chip U3 has an own watchdog timer and a comparator for the creation of a interrupt signal /PFO.

8.1 The External Watchdog-Timer

The SAB80C537 has already an internal watchdog-timer, but in some cases an external watchdog timer might be advantageous:

For applications where the time constant of the watchdog timer is too small and for applications, where an external signal must be monitored.

The controller watchdog reacts only to a program crash or error of the clock. The additional watchdog timer in U3 allows the reaction to external events and is activated by a cyclic application of a low level to A62 (/WDI). If the signal fails for an adjustable period, the system is reset. The external watchdog remains inactive as long as A62 is not connected. The time constant is within the period of one to two seconds.

8.2 The Watchdog- and RESET-Time-Base

When the signal inputs OSC_SEL and OSC_IN are not connected, the RESET-pulse has a duration of 50msec and the watchdog-timer reacts after 1.6 sec. To change the timing the following options are possible:

Set JP1 (OSC_SEL)

As long as OSC_SEL is open or HIGH, the internal oscillator determines the timing of U3. If VCC or GND is connected with OSC_IN the internal cycle can be changed.

The exact description of the monitor chip would exceed this documentation. Please use the corresponding data sheets of this chip or ask us in case of problems.

8.3 Application of the Power-Fail-Input (PFI

The power-fail-input allows the premature recognition of power failures. For this reason the uncontrolled voltage should be connected to A39 (PFI) from the power supply with an appropriate voltage divider before or at a sufficient high load capacitor. The power-fail-input of the monitor chip compares the applied voltage with an internal reference voltage of 1.3 V. The dimensioning of the voltage divider is up to you. If the supply voltage is decreasing below the computed value, the signal /PFO goes LOW and can save data with an interrupt. The PFI-interrupt can be achieved with /INTO or with /INT1. For this purpose external connections might be required.

9 A/D Converter of the SAB80C537

The internal A/D converter of this controller is a real 8-bit converter. The twelve analog inputs are switched by an 12:1 analog multiplexer. The converter has the feature that the conversion range for 8-bit resolution is programmable in ratios of the external applied reference voltage. The minimal size of the conversion window should not be less than 1 V.

The converter of the SAB80C537 is very suitable for many applications, but doesn't replace a converter of high precision. For your applications consider, if the specifications of the converter from INFINEON satisfies your expectation. An additional external converter chip is easily connected to the miniMODUL-537.

The external reference voltage VAREF and VAGND are close to VCC and GND. Intermediate values are not permitted. The converter does not operate without external reference voltages VAREF and VAGND. The reference voltages have to be connected to the analog connecting stripe C. The handling of the integrated A/D converter of the 80C537 is compatible to the 80C535. The connections for this purpose are SFR, ADDAT, ADCON0, ADCON1 and DAPR. ADCON0 corresponds to the SFR ADCON of the 80C535. ADCON1 is used to select the twelve analog inputs. The software of the 80C535 will operate the lower eight channels correctly.

As already mentioned, the informations concerning the accuracy of the converter are found in the INFINEON controller manual. Since the SAB80C537 doesn't provide the feature of nullification, a zero deviation has to be considered. This error can be compensated by software or by adjustment of the input-amplifiers, which are often employed.

10 The RESET-Signal

To avoid the disadvantages of plain RESET circuits, the watchdog-timer U3 was used, without restricting the utilization of the timer otherwise.

To trigger a RESET-pulse the RESET-contact has to be pushed for about 5 seconds.

For user circuit extensions the available RESET signals are not meaningless:

/RES
The output /RES of U3 is active low and should not be loaded too much, because otherwise the slope of the pulse edge might be decreasing and the Power-On-Jump and the RAM write-protection might not operate appropriately anymore. /RES is an open-drain output and can be connected to GND externally. However this is not used here.

RES
The RES-output of U3 is active high and can be loaded more. The load has no influence to the monitor-chip U3. The output is only defined as long as VCC is within the allowed range.

B-RES
This output is active HIGH. This output functions similarly like RES, but always provides the reverse of /RES. B-RES always has the battery voltage for an active status, provided a battery is connected. Therefore this output is also appropriate for controlling extensions without the supply voltage VCC.

11 The Optional Real-Time-Clock RTC72421

The optional Real-Time Clock always operates with battery voltage, independent of the function of the miniMODUL-537. The clock-crystal is already integrated, so that a tuning is not necessary. The clock has a 4-bit interface for the connection to the processor-bus. The miniMODUL doesn't provide an address decoder to select the clock.

11.1 Selection of the RTC

The clock is already completely connected to the processor-bus, except the /CE-connection A59. In order to select the clock either an external address decoder or two vacant port lines have to be used. Hereby the clock can be used with minimal expenditure without address decoder.

Writing to the Clock

The RTC is selected the whole time until the writing is finished by the connection of A59 to a port line. The RAM is also selected at the same time and therefore a partition of the address region has to be selected, which is not used otherwise.

Reading from the Clock

The RTC is also selected the whole time, but the RAM is masked outside with the module-connection M-DIS (A11). For this purpose an additional second port line is required, which is connected with A11. Don't forget in this case to disconnect JP5, which is already connected.

11.2 Programming of the Clock

By data-access to the different clock registers the time and the date can be programmed. In addition there are the options like USA time, clock start/stop and second-, hour- or day pulses for processor interrupts.

The addresses of the separate clock registers can be taken from the register table of the data sheet from the RTC.

11.3 The Standard Pulse-Option

The RTC has a pulse-output. This is a N-channel-FET connected to GND. This output provides periodical pulses, which are programmed by the bits t1 and t0. The pulse can be turned off by a bit mask. The frequencies of the pulse can be depicted from the following table.

t1	**t0**	**Pulse frequency**
0	0	1/64 second
0	1	1 second
1	0	1 minute
1	1	1 hour

The duration of one pulse is 7.8125 msec.

11.4 Description of the Control-Bits

The exact description of the RTC would exceed the scope of this documentation. Please use the corresponding data sheets of this chip or ask us in case of problems.

HOLD
HOLD has to be set immediately before the access of the time/date registers. After termination of all write or read accesses, HOLD has to be disabled again.

This operation should take place within one second.

BUSY
This bit can be read only. Access to registers should take place only if BUSY is LOW. BUSY is always HIGH, when HOLD is not HIGH. After setting of HOLD , BUSY is LOW at the latest after 190 µsec.

MASK
This bit prevents the LOW level at the pulse-output, when it is enabled. For the application with standard pulse, MASK has to be erased.

ITRPT/STND
This bit selects the pulse-output between interrupt-mode and fixed-mode. The interrupt mode is not described here. This bit should be LOW. This results in the fixed-pulse mode with a duration of 7.8123 msec.

REST
This bit is set to erase the counter of the second-ratios. The ratio counter is on hold, as long as REST is HIGH. The counter must be enabled by erasing this bit.

STOP
Setting STOP stops the counter completely. The clock starts at the latest 122 µsec after erasing this bit.

24/12
This bit determines the upper limit of the hour display. HIGH sets the 24-hour cycle, LOW the 12-hour cycle. In the 24-hour cycle the PM-bit is ineffective. Nevertheless this bit should be masked out. Manipulating this bit should always be combined with setting the REST-bit. In the 24-hour mode the bit sequence '0101' and '0100' should be set and in the 12-hour-mode the bit sequence '0001' and '0000' should be in the register F.

TEST
This bit must be erased.

More detailed information should be taken from the data sheets of the clock chip.

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